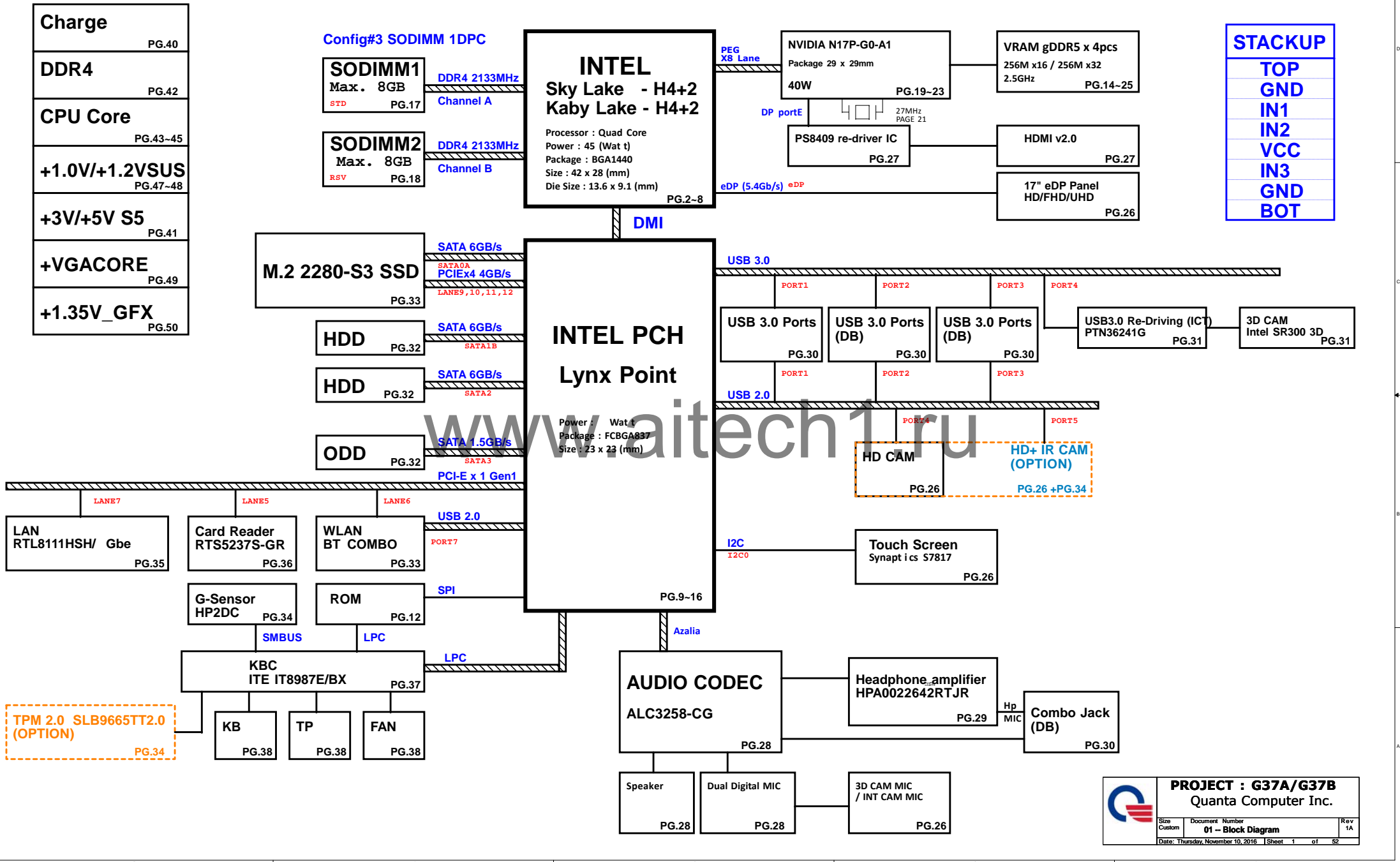
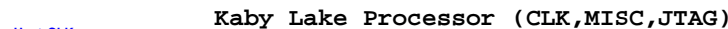
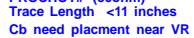


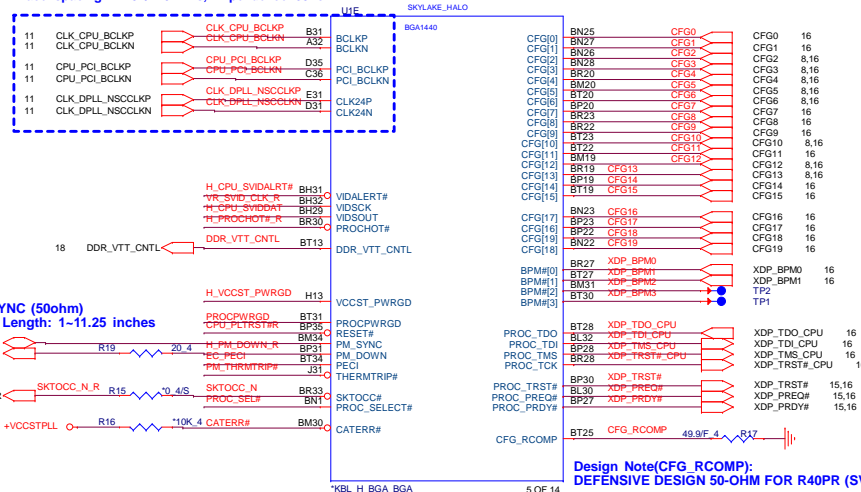
POWER PAVILION PARFAIT INTEL SKL / KABY -H SYSTEM DIAGRAM 01



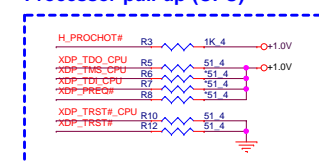
Trace Length: <0.5 inches
Ra,Ca need placement close to PCH.



Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impedence 85 ohm



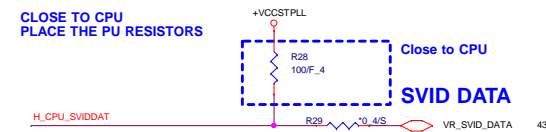
Processor pull-up (CPU)



CPU CORE SVID

Layout note:

- Layout note:
1. Need routing together
2. ALERT need between CLK and DATA.

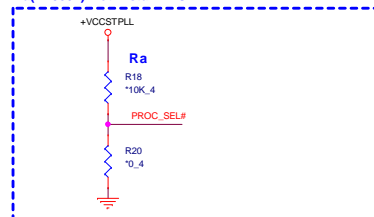


PROCPWRGD (50ohm)

Trace Length: 1~11.25 inches

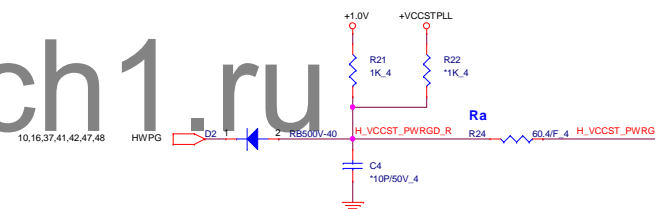


Trace Length: 1.1~12 inches
Rb need placment near PCH



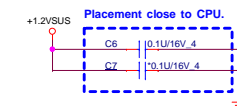
HWPD

Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



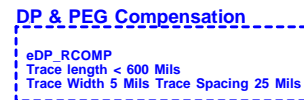
CPU VDDQ

Note: please keep plane is enough for VDDQ 2.8A

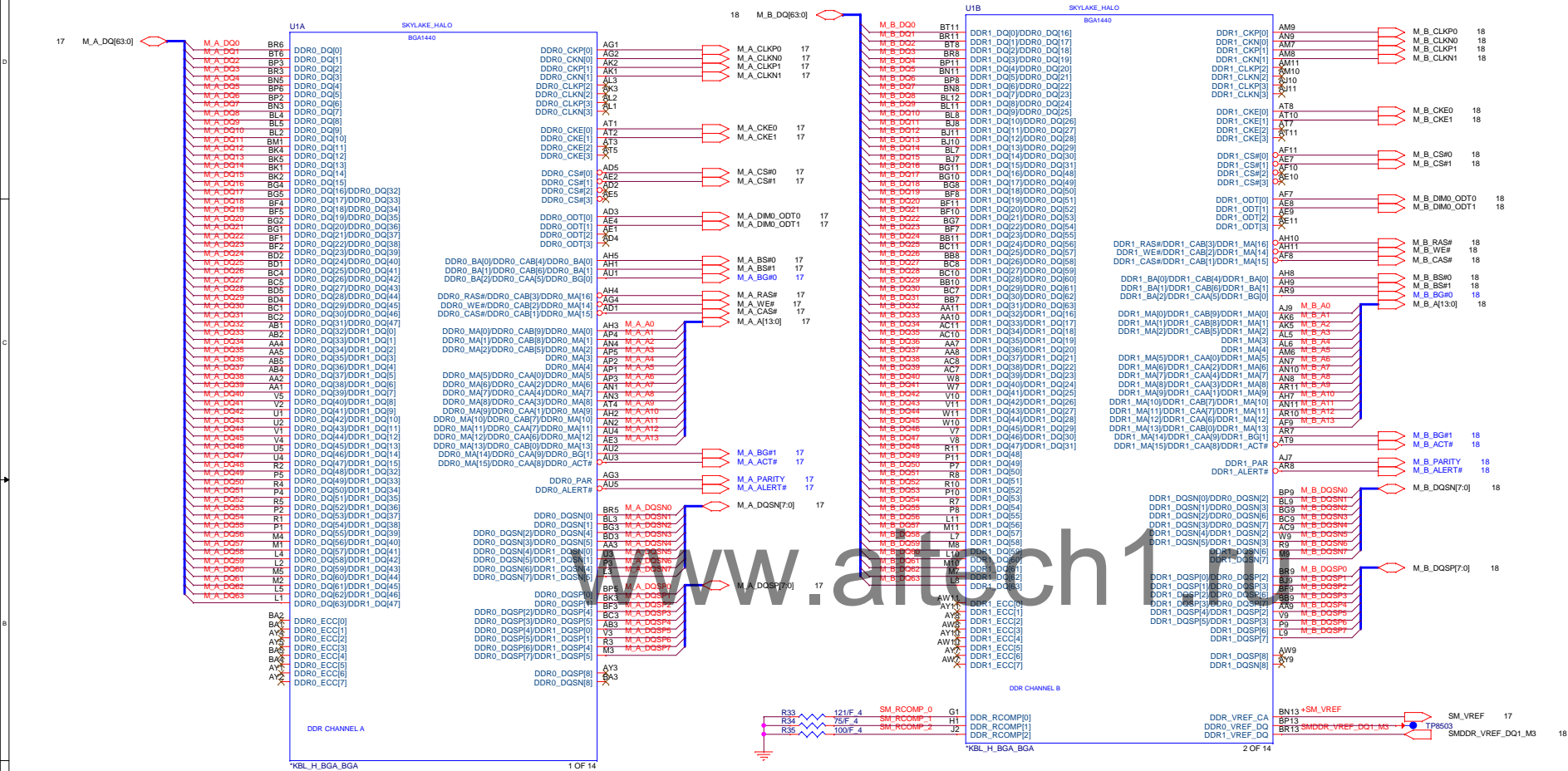
**PROJECT : G37A/G37B**

Quanta Computer Inc.

Size Custom	Document Number 02 -- SKL 1/7 (JTAG/MISC)	
Date: Thursday, November 10, 2016	Sheet	2 of 5



Kaby Lake Processor (DDR4)

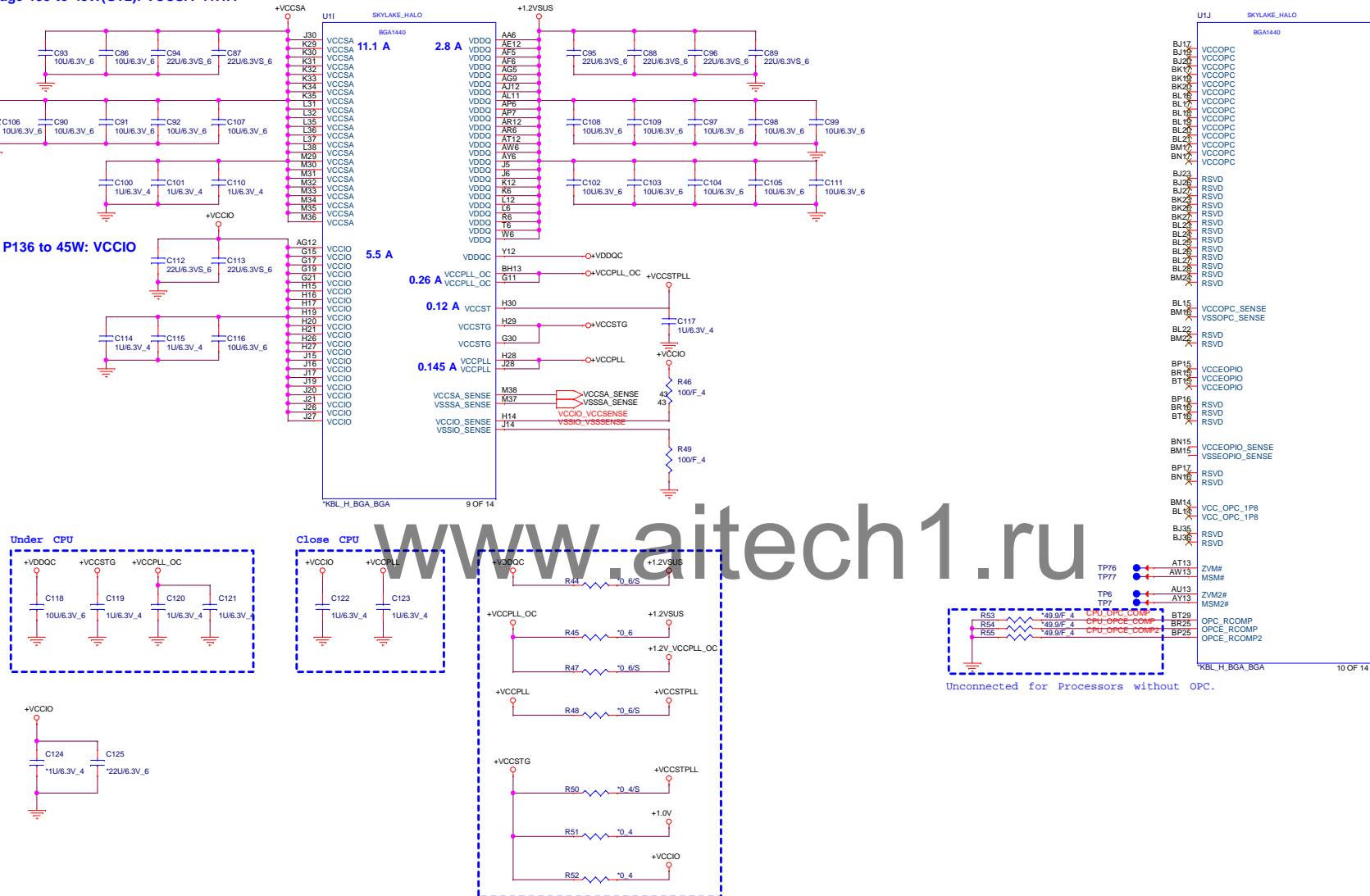


+1.2VSUS 2,10,17,18,42,48,51
 +VCCIO 3,16,48
 +VCCSTPLL 2,43,47
 +VCCSA 43,45

Follow SKL H EDS page 135 to 45W(GT2): VCCSA=11.1A

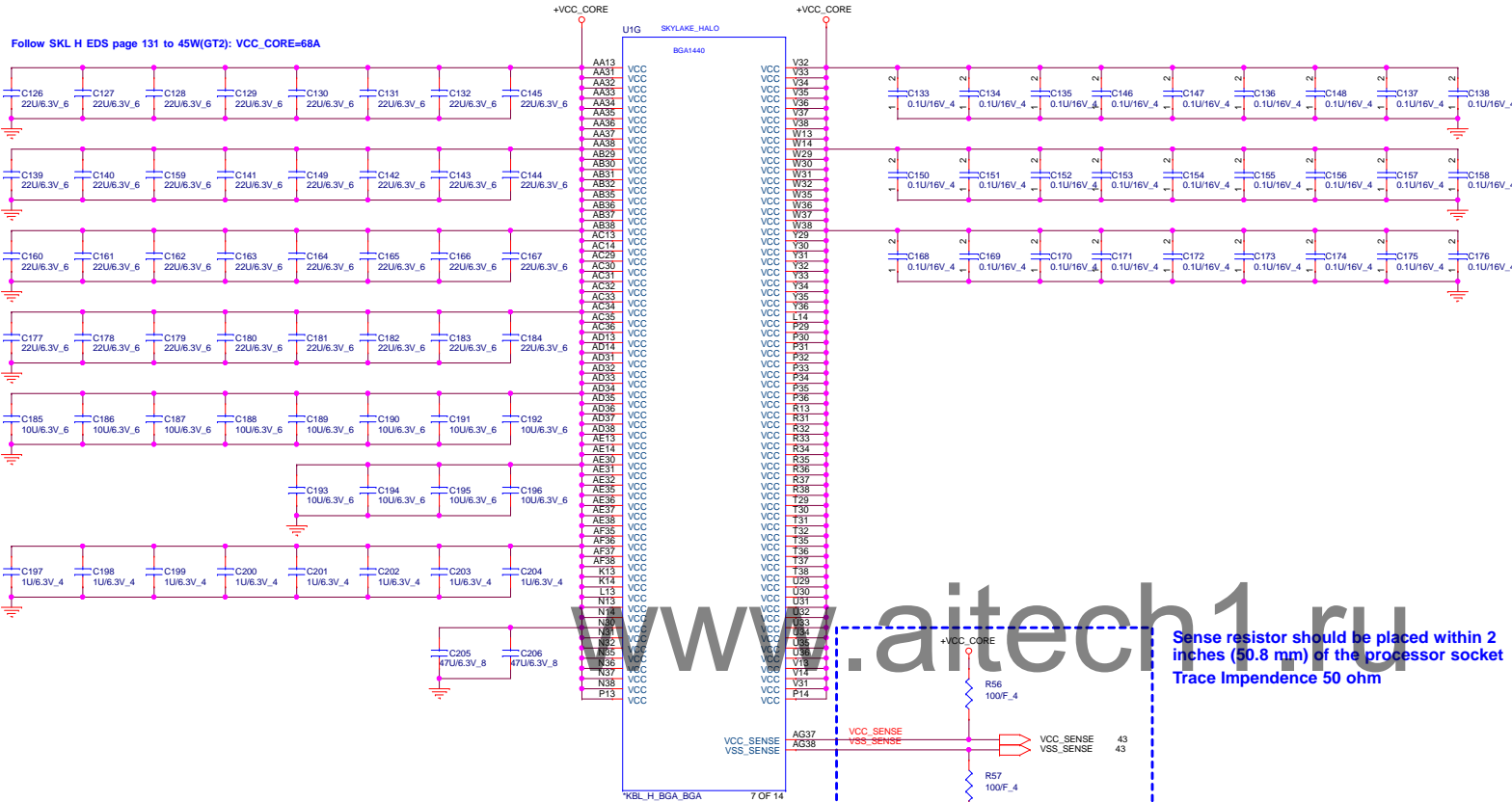
Follow SKL H EDS page 135 45W: VDDQ=2.8A

Follow SKL H EDS P136 to 45W: VCCIO
+VCCIO = 0.95V



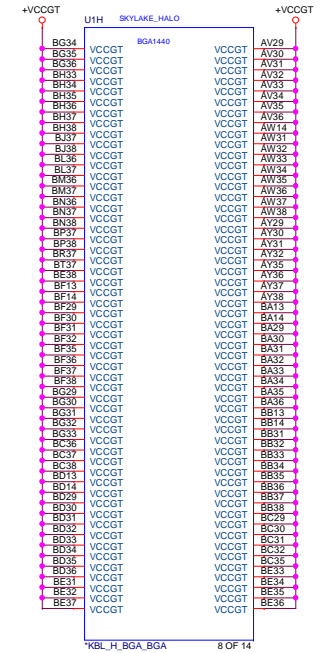
+VCC_CORE 44
+VCCGT 5,43,45

Follow SKL H EDS page 131 to 45W(GT2): VCC_CORE=68A

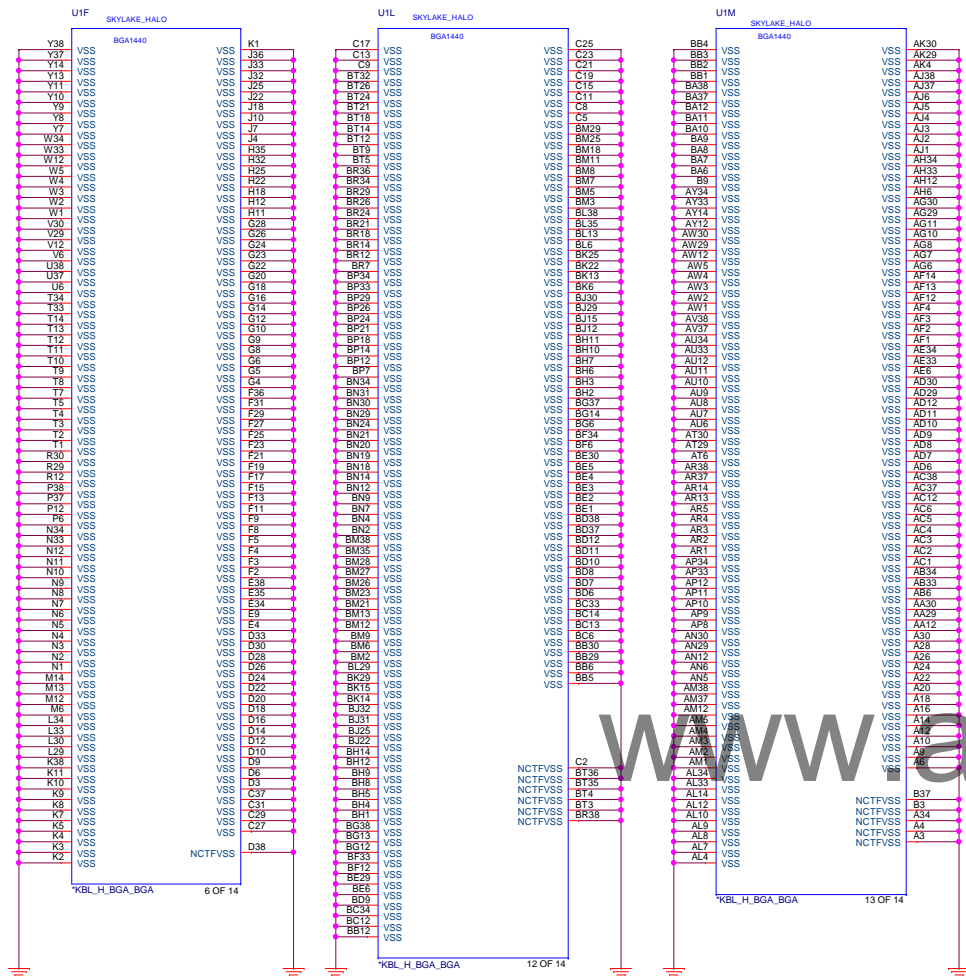


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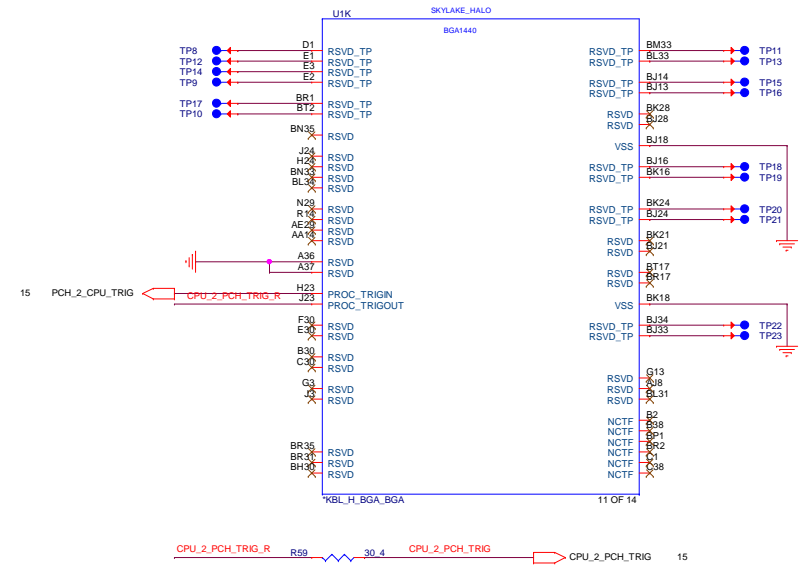
Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket
Trace Impedance 50 ohm



KBL-HProcessor (GND)



KBL-H Processor (RESERVED, CFG)

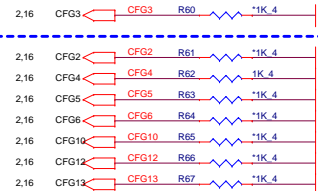



Processor Strapping

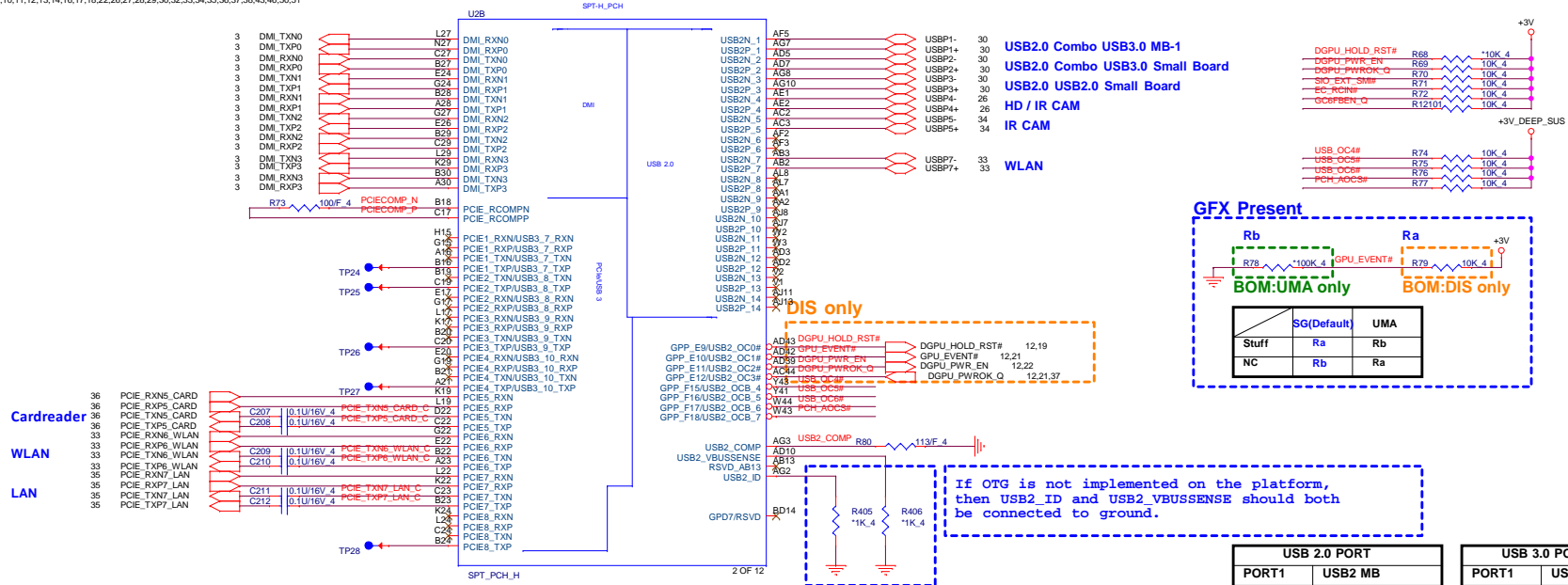
The CFG signals have a default value of '1' if not terminated on the board

0 Enable; SET DFX ENABLED BIT IN DEBUG

1 , Disable;

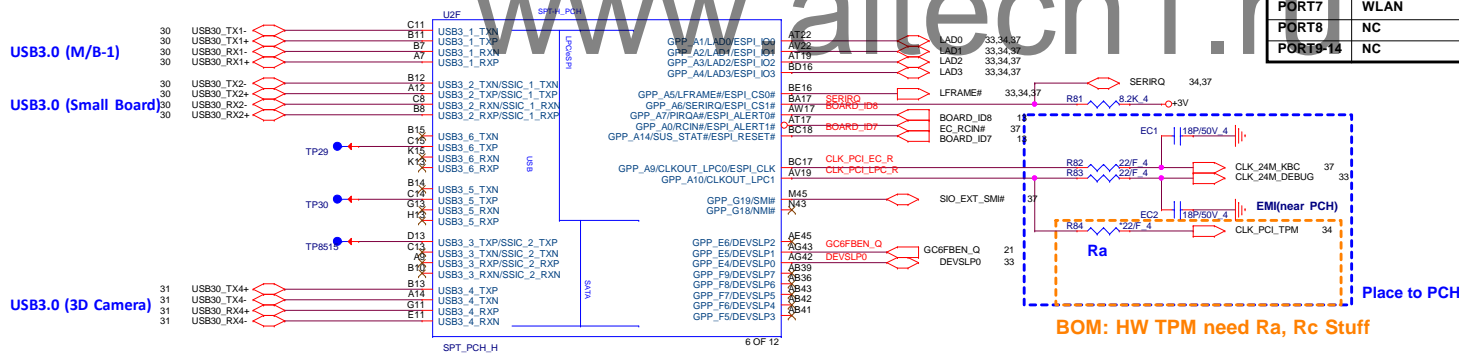


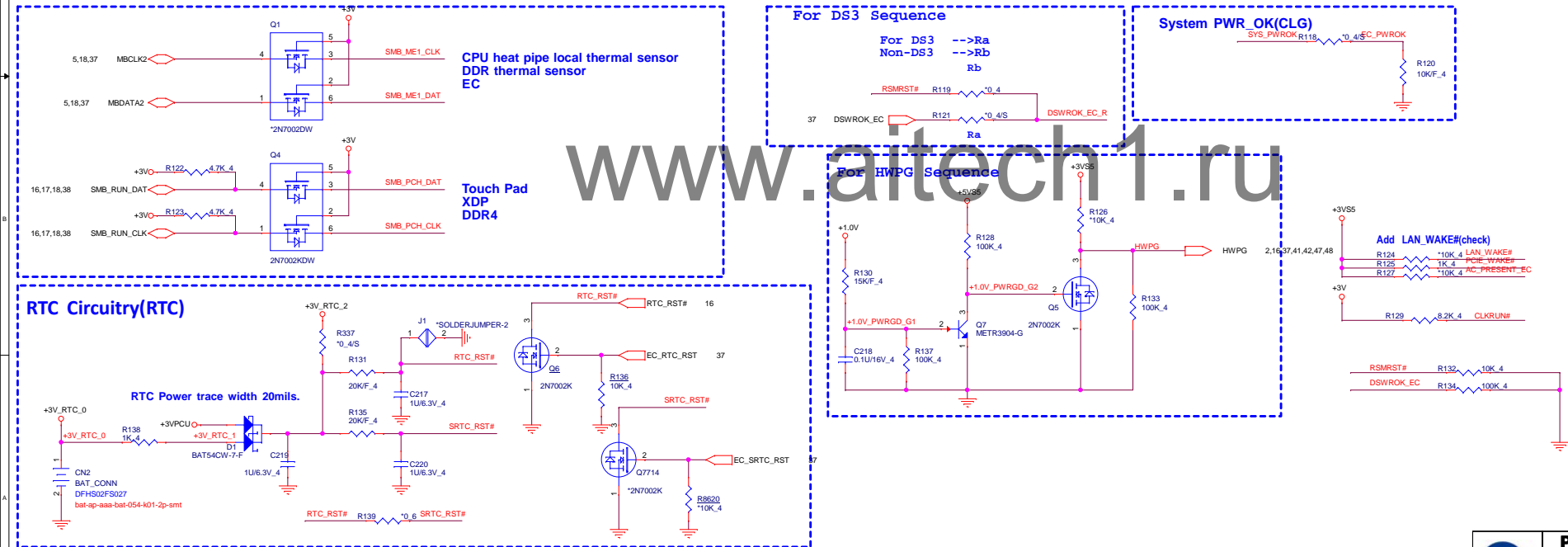

 +3V_DEEP_SUS 10,12,13,14,16,18
 +3V 5,10,11,12,13,14,16,17,18,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,50,51



USB 2.0 PORT	
PORT1	USB2 MB
PORT2	USB2 DB
PORT3	USB2 DB
PORT4	HD I/R CAM (OPTION)
PORT5	IR CAM (OPTION)
PORT6	NC
PORT7	WLAN
PORT8	NC
PORT9-14	NC

USB 3.0 PORT	
PORT1	USB3 MB
PORT2	USB3 DB
PORT3	NC
PORT4	3D CAMER





+3V 5.9,10,12,13,14,16,17,18,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,50,51
+1.0V_DEEP_SUS 10,14,16,47,48

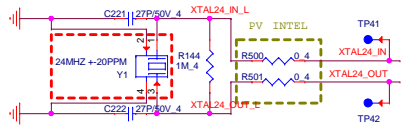
HSIO MUX PORT	
PCIE1-4	NC
PCIE5	Cardreader
PCIE6	Wlan
PCIE7	Lan
PCIE8	NC
PCIE9/SATA0A	
PCIE10	SSD PCIE x 4
PCIE11	
PCIE12	
PCIE13	NC
PCIE14	HDD-1
PCIE15	HDD-2
PCIE16	ODD
PCIE17	NC
PCIE18-20	NC

SSD PCIE x4 LANE

HDD-1 (SATA1B 6Gb/s)

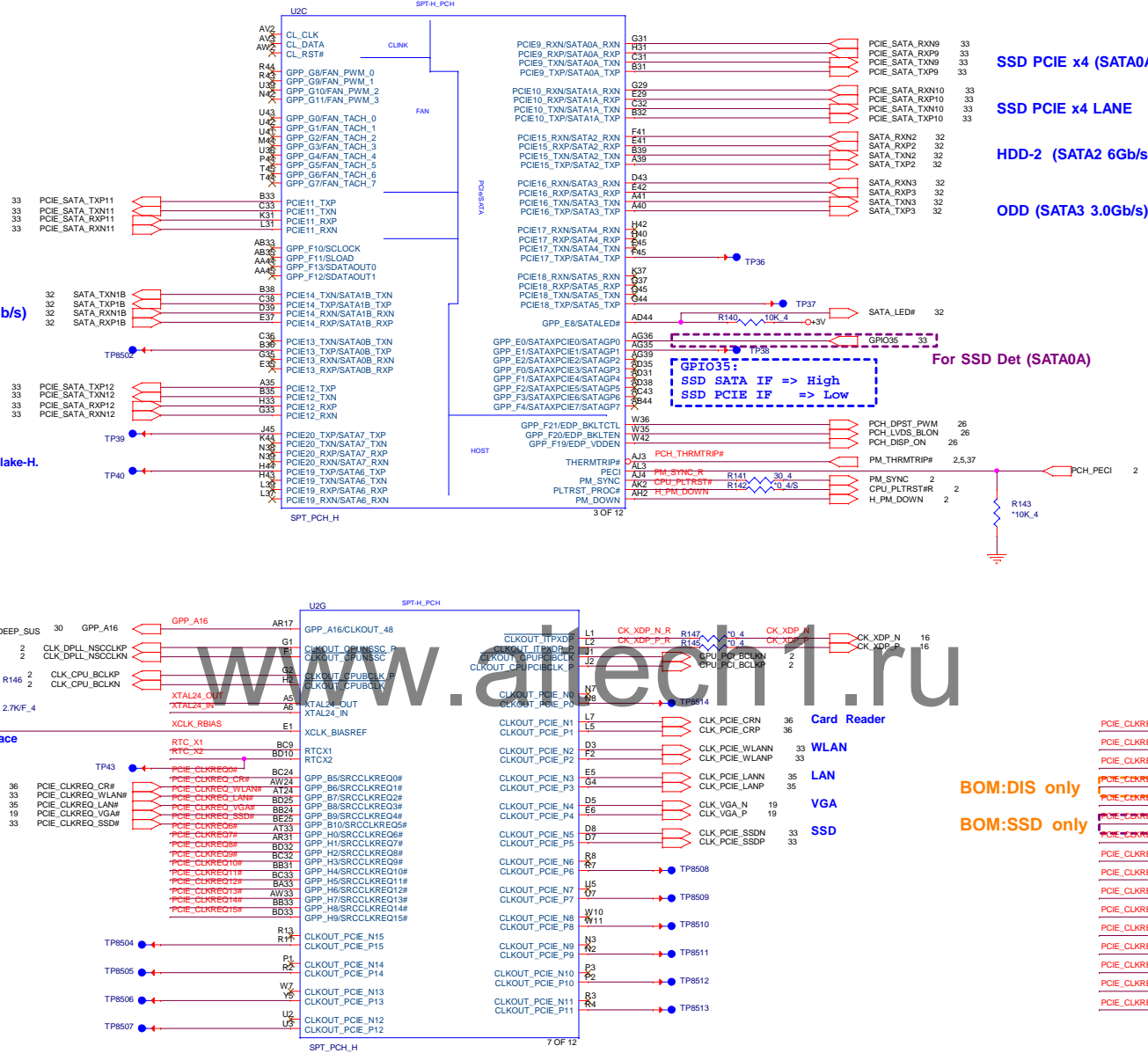
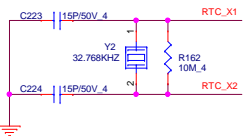
SSD PCIE x4 LANE

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-H needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-H.



Crystal Components with Surrounding 10 mil Wide GND Shield Trace
Break Out: 4-10 mil Wide GND Shield Trace

RTC Clock 32.768KHz



SSD PCIE x4 (SATA0A) LANE

SSD PCIE x4 LANE

HDD-2 (SATA2 6Gb/s)

ODD (SATA3 3.0Gb/s)

For SSD Det (SATA0A)

BOM:SSD only

BOM:DIS only

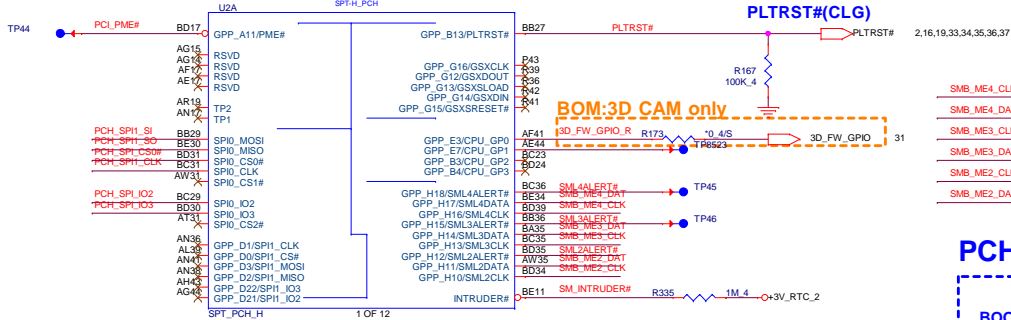
BOM:SSD only



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Size	Document Number	Rev
Custom	11 - PCH 3/7 (SATA/LPC/CLK)	1A
Date:	Thursday, November 10, 2016	Sheet 11 of 52

+3V_RTC_2 10,14
 +3V5 10,14,16,33,37,41,42,46,47,48
 +3V_DEEP_SUS 9,10,13,14,16,18
 +3V 5,9,10,11,13,14,16,17,18,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,50,51

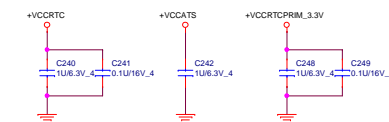


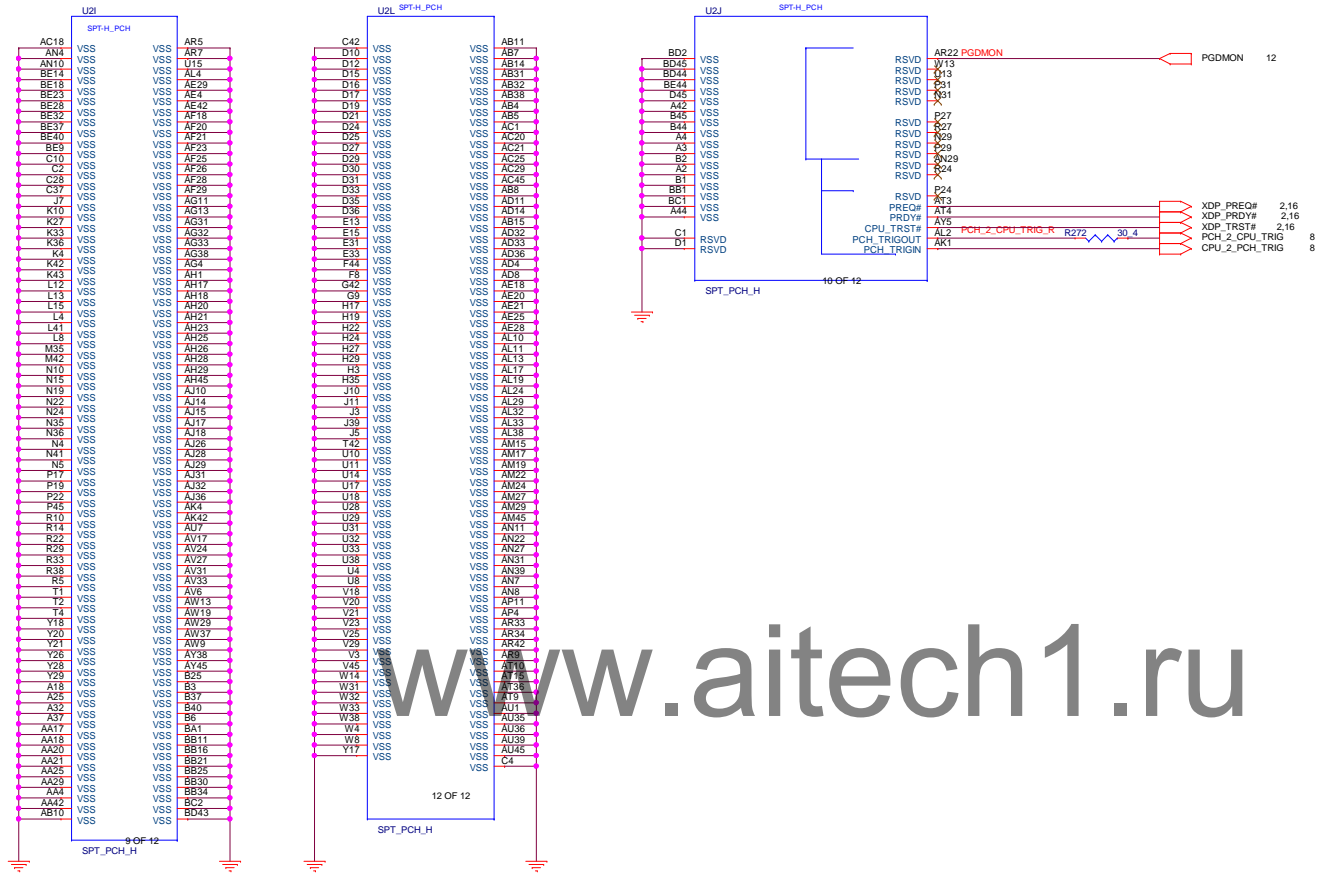
BOM
final decide to use "01" for SKL-H

Model	BOARD_ID[8:7] ID8;ID7	BOARD_ID[6:5] ID6;ID5	Board ID [4:3] ID4;ID3	BOARD_ID[2:1] ID2;ID1	BOARD_ID[0] ID0
Definition	00 Non 3D CAM 01 3D CAM	00 Reserved	Reserved	00 15" P SKL H 01 17" P SKL H 10 17" SP SKL H 11 17" KBL H	0 : U M A 1 : D S

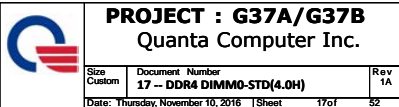
- This signal has a weak internal pull-down
- 0 = Port C and D is not detected.
- 1 = Port C and D is detected.

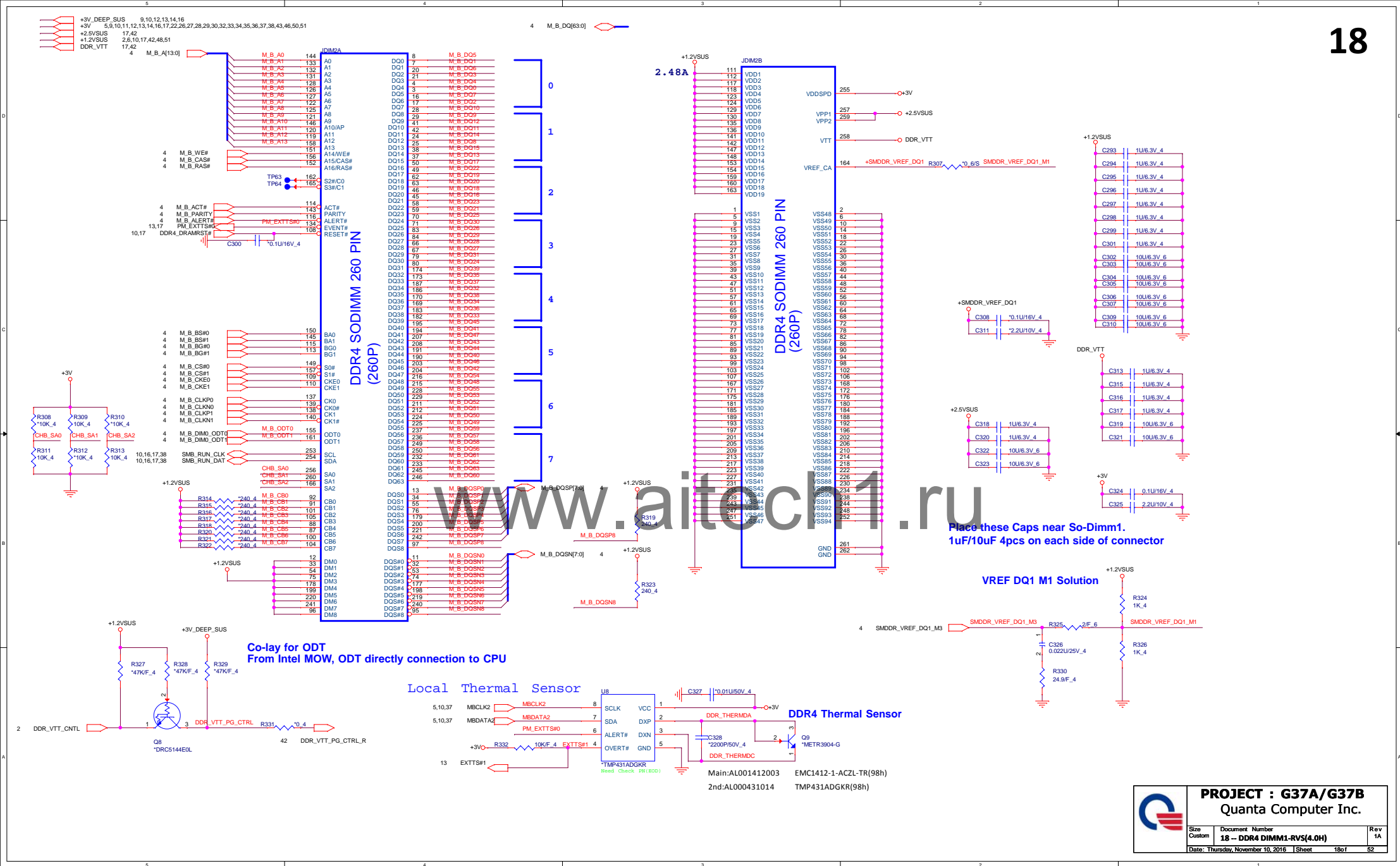
12/28 SDVO_DATA pulled up through a 2.2KΩ ± 5% pull - up to 3.3V for Panel brightness without control issue

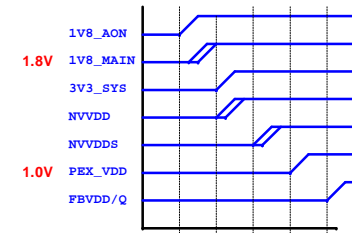




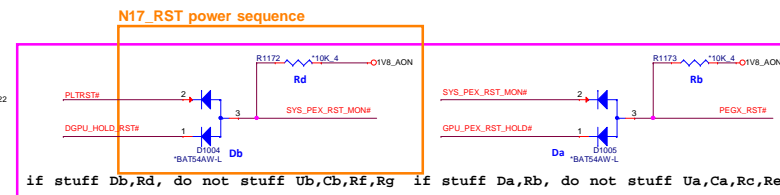


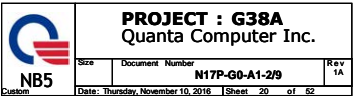


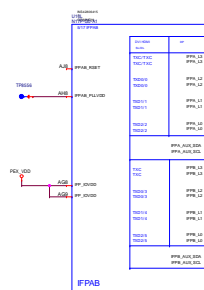




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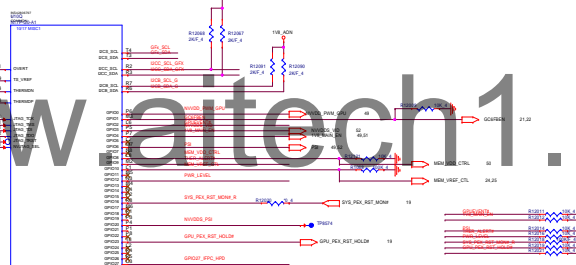
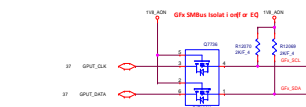


STRAP[2:0] VRAM Table for N17P-G0 GDDR5 Recommended Memories

STRAP[2:0]	DESCRIPTION	Vendor	Vendor PN	TOP P/N	OS P/N	Default
Str0	GDDR5 256Mx32 7 GHz	SamSung B die	K4D513238E-1028	AKGSG00D1508	AKGSG00D1508	
Str1	GDDR5 256Mx32 7 GHz	Metrix A die	M512358K3382-701A	AKGSG00D1507	AKGSG00D1508	
Str2	GDDR5 256Mx32 7 GHz	Hynix A die	H5GQ8324A28-B0C			
Str3	GDDR5 128Mx32 7 GHz	SamSung E die	K4D413238E-1028	AKGSG00D1501	AKGSG00D1502	
Str4	GDDR5 128Mx32 7 GHz	Metrix A die	K2M413238B3-70-P-JR	AKGSG00D1508	AKGSG00D1507	
Str5	GDDR5 128Mx32 7 GHz	Hynix A die	H5GQ4824A28-B0C	AKGSG00D1506	AKGSG00D1505	

Vendor	Size	PN
NTE-DX	WBG000	8MB
NTE-DY	Giga device	1Mb

AKSEZNIN08 (W204PWS00)



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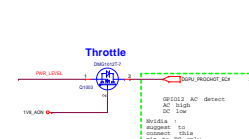
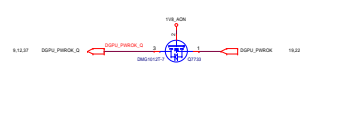
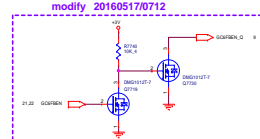


Table 14.2 GPIO Descriptions for GB4C-128 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	HWPGD_PWD_VID	O	Pin0 Output to control HWPGD	0 to V18_PWD output
GPIO1	GCMAI_GCK_P8_DI	O	FB Enable for GCK 2.1	Open Source 10 kΩ pull-down
GPIO2	GCMAI_GPU_RESET	I	GPU reset signal for GCK 2.1	100 kΩ pull-up to V18_ACH, unless driven actively
GPIO3	HWPGD_STAN_PWD	O	Pin0 output to control the STAN power supply	0 to V18 output
GPIO4	GCMAI_HAR_PWD	O	GPU power sequencing for GCK 2.1	Open Drain 100 kΩ pull-up to V18_ACH
GPIO5	PWR_LCK	I	Active low Frame Lock	Open Drain 100 kΩ pull-up to V18_ACH

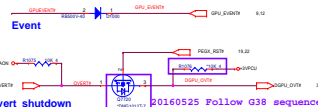
Table 14.3 GPIO Descriptions for GB4C-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO6	HWPGD_P8	O	Phase Shedding (see Section 14.3.3)	10 kΩ pull-up to V18_ACH to enable multiple phases
GPIO7	LED_BL_PWD	O	Panel Backlight enable	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pin up/pull-up to V18_ACH to set the V18_ACH power supply to V18_PWD
GPIO9	TRNG_ALERT	I/O	Active Low Thermal Alert	Open Drain 100 kΩ pull-up to V18_ACH
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LED_VDD	O	Quadro Power enable	100 kΩ pull-down
GPIO12	PWR_LEVEL	I	Power level detect	100 kΩ pull-up to V18_ACH
GPIO13	LED_BLEND	O	LED Blend Enable	Panel Backlight Enable
GPIO14	HPD_P8A	I	Hot Plug Detect for P8A	Inverted input. See Figure 14.3
GPIO15	HPD_P8B	I	Hot Plug Detect for P8B	Inverted input. See Figure 14.3
GPIO16	GCMAI_P8_RST_ACH	O	System side PCIe reset monitor	10 kΩ pull-up to V18_ACH unless actively driven
GPIO17	HPD_P8D	I	Hot Plug Detect for P8D	Inverted input. See Figure 14.3
GPIO18	HPD_P8E	I	Hot Plug Detect for P8E	Inverted input. See Figure 14.3
GPIO19	SD_VIDEN	O	SD Video I/O Signal	100 kΩ pull-down
GPIO20	HPD_P8F	I	Hot Plug Detect for P8F	Inverted input. See Figure 14.3
GPIO21	UNLCKED	I/O		
GPIO22	UNLCKED	I/O		

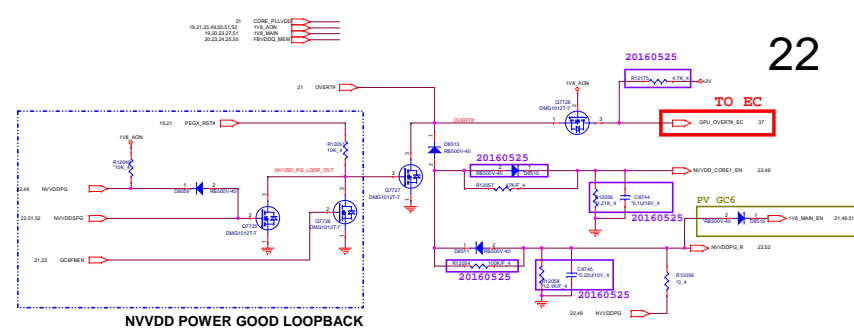
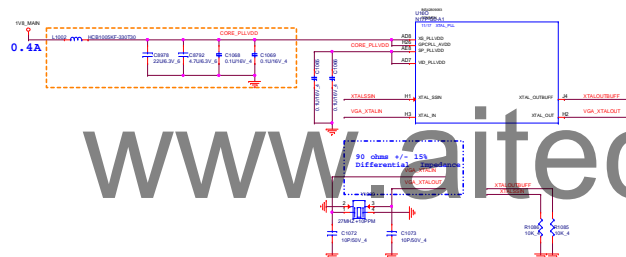
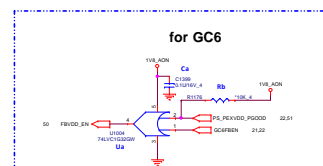
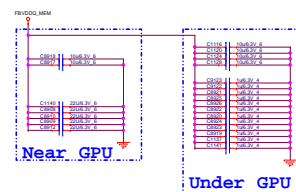
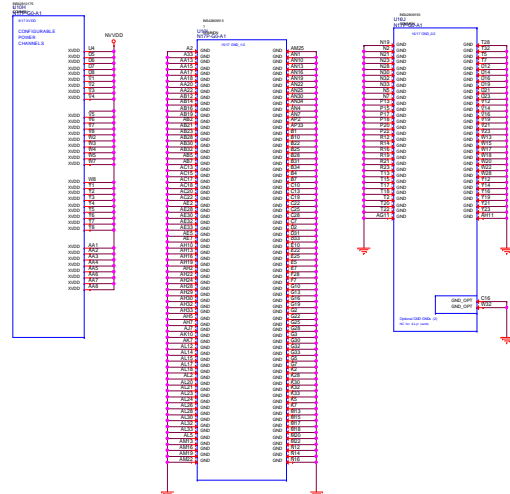
Table 14.2 GPIO Descriptions for GB4C-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO23	GCMAI_GPU_RESET_HOLD	O	GPU PCIe self-reset control	Open Drain 10 kΩ pull-up to V18_ACH
GPIO24	HPD_P8G	I	Hot plug detect for P8G	Inverted input. See Figure 14.3
GPIO25	UNLCKED	I/O		
GPIO26	UNLCKED	I/O		
GPIO27	HPD_P8H	I	Hot plug detect for P8H	Inverted input. See Figure 14.3

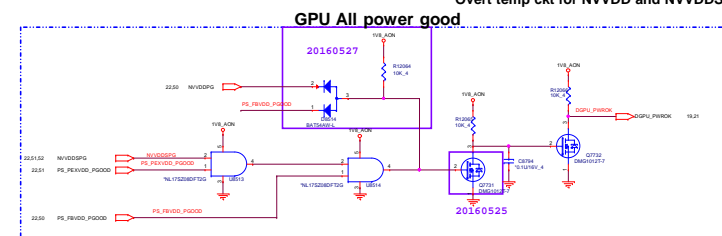
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO28	CHTERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to V18_ACH



Overt shutdown 20160525 Follow G38 sequence

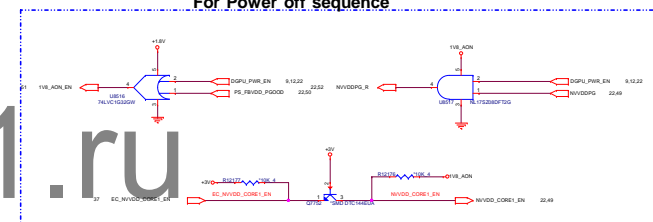


NVDD POWER GOOD LOOPBACK



Overt temp ckt for NVDD and NVVDDs

For Power off sequence





Channel 1
<32-63>

MF=0 Non-mirrored

MF=1 mirrored FBVD

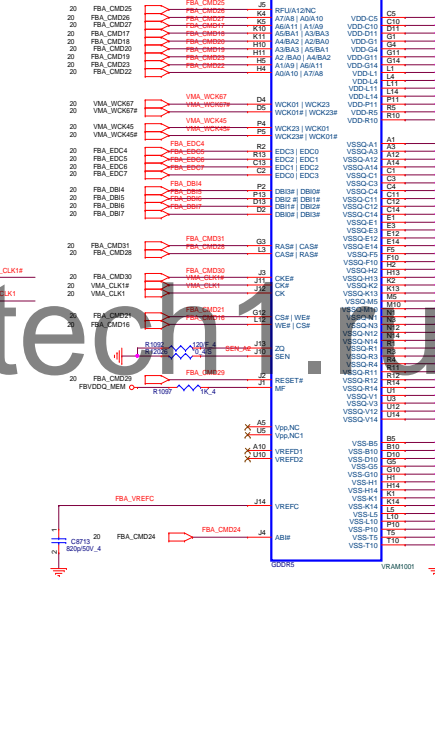
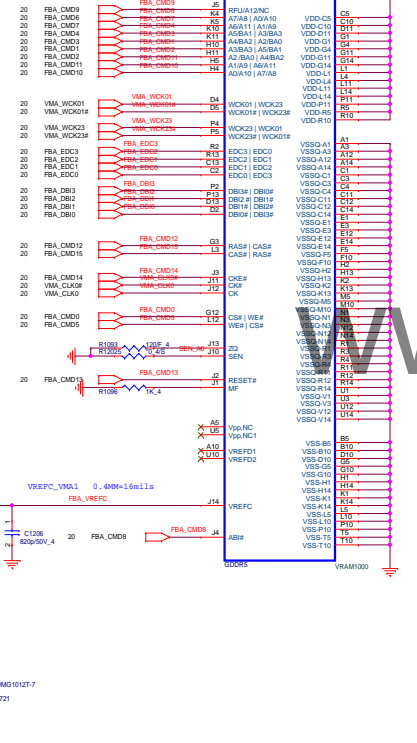
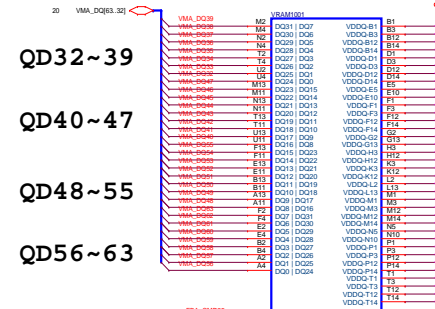
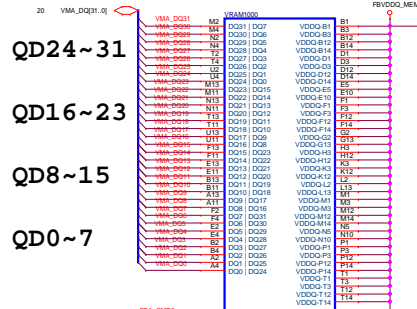
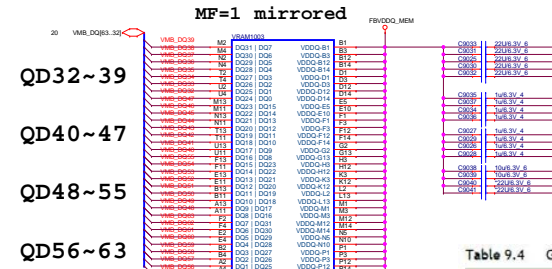


Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	AB*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

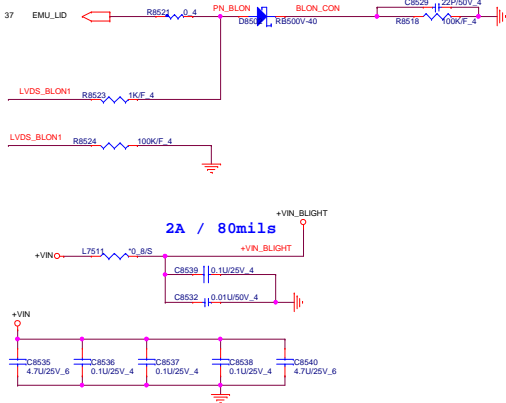


Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	AB1*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RS1*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

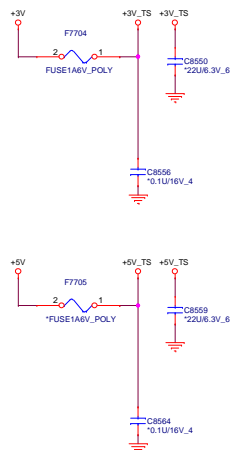
Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

+VIN 32,38,39,40,41,42,43,44,45,46,47,48,49,50,52
 +5V55 10,28,30,41,42,43,44,45,46,47,48,49,50,51,52
 +5V 27,28,29,32,38,46,49
 +3V55 10,12,14,16,33,37,41,42,46,47,48
 +3V 5,9,10,11,12,13,14,16,17,18,22,27,28,29,30,32,33,34,35,36,37,38,43,46,50,51
 +3V_CAM -34

LID Switch



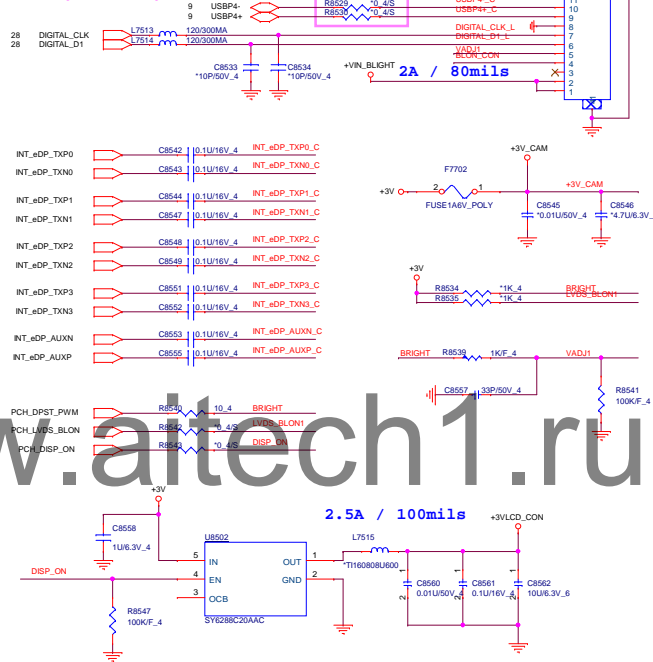
Touch screen




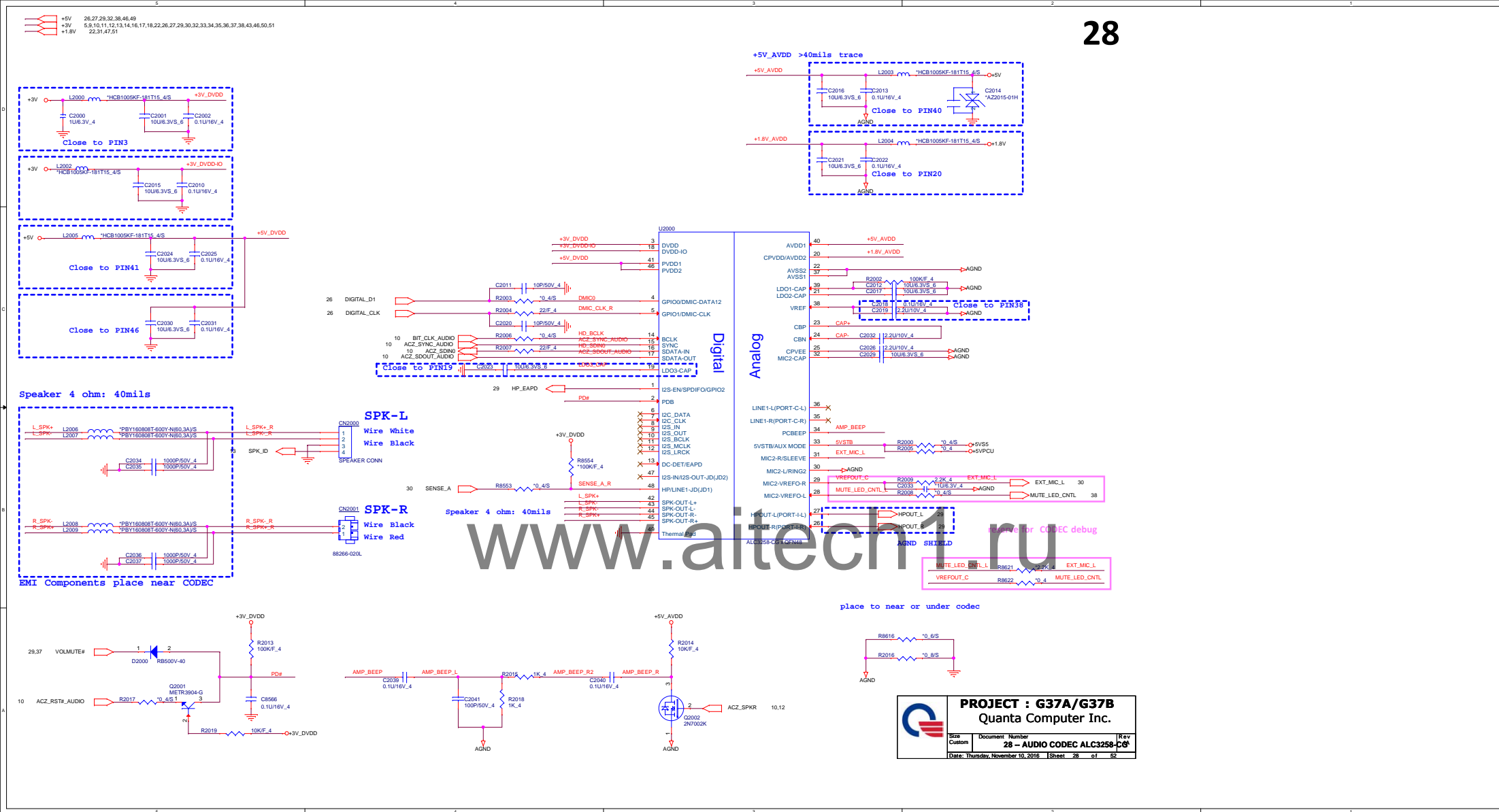
eDP Conn.

MB	TS (I/F: I2C)
+3V_TS	VDD33
I2C_DATA_TS	SDA
I2C_CLK_TS	SCL
TCH_PNL_RST#_EC	EXRESETN
TCH_PNL_INT#	ATTN
TS_ON	Report_Switch
GND	GND

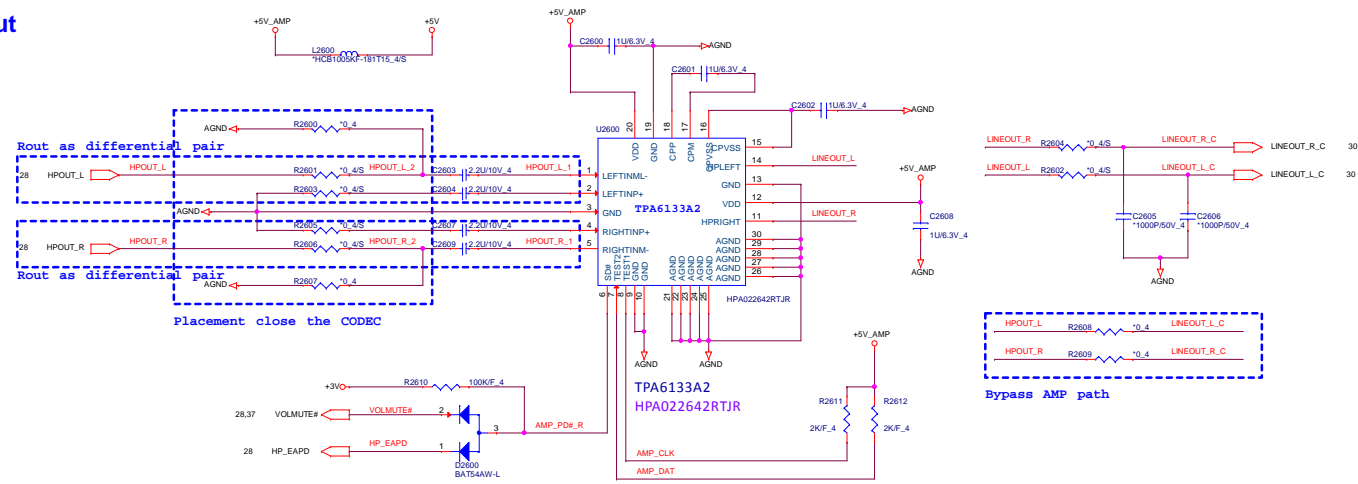
3/9:3D CAM/HD CAM combine




PROJECT : G37A/G37B
Quanta Computer Inc.
 Size Custom Document Number
27 -- HDMI/HDMI REDRIVER
 Date: Thursday, November 04, 2016 1:58 PM Page 23 of 23



Head Phone out

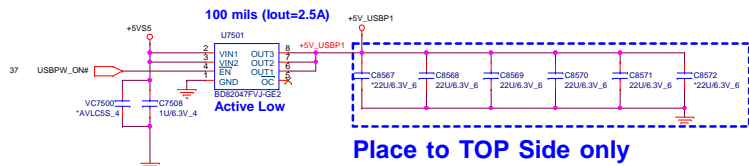


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PROJECT : G37A/G37B
 Quanta Computer Inc.

Size	Document Number	Rev
Custom	29- HP AMP HPA022642RTJR	1A
Date: Thursday, November 10, 2016	Sheet 29 of 52	

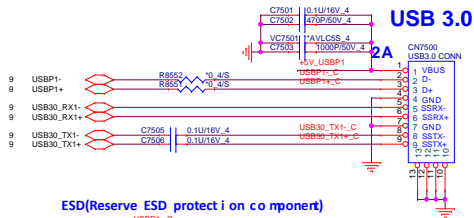
+5VSS	10,28,41,42,43,44,45,46,47,48,49,50,51,52
+5VPCU	5,10,21,33,37,38,40,41
+3V	5,9,10,11,12,13,14,16,17,18,22,26,27,28,29,32,33,34,35,36,37,38,43,46,50,51
+1.8V	22,28,31,47,51



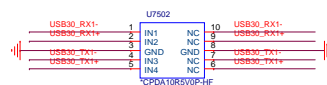
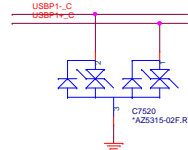
Place to TOP Side only

USB 2.0/3.0 Combo

30

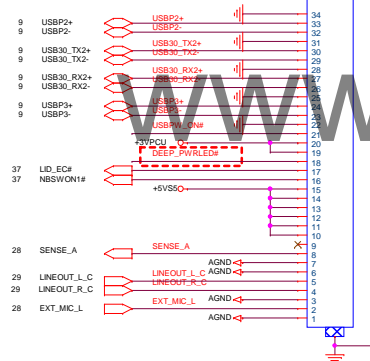


ESD(Reserve ESD protect i on c o mponent)

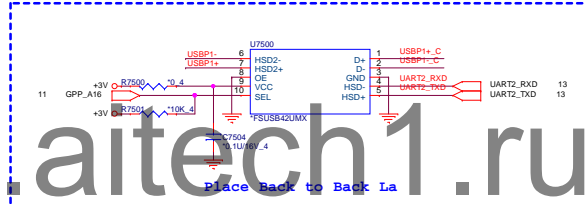


Daughter Board

51619-03401-001
51619-03401-001-34p-I
DFPC34FR030
CN7702

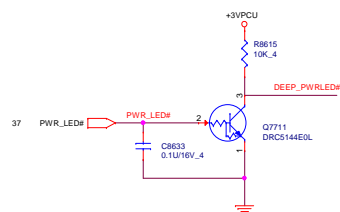


UART for Win7 WHQL DEBUG



Place Back to Back Ia

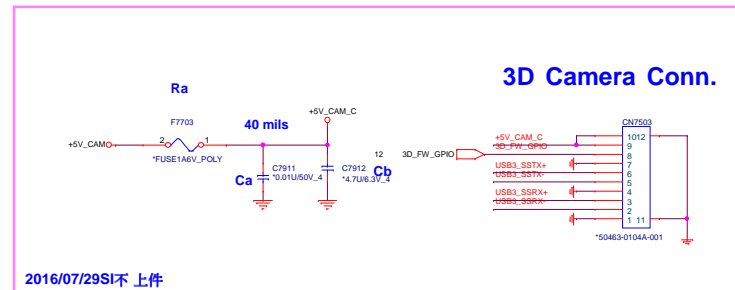
PWR LED MOS Circuit



	PROJECT : G37A/G37B	
	Quanta Computer Inc.	
Size	Document Number	Rev
Custom	30 - USB3.0/DB	1A
Date: Thursday, November 10, 2016	Sheet 30 of 52	

+5V 26,27,28,29,32,38,46,49
+3VPCU 5,10,21,30,33,37,38,40,41
+3V 5,8,10,11,12,13,14,16,17,18,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,50,51
+1.8V 22,28,47,51

BOM: 3D CAM/HD CAM combine



BOM: 3D CAM/HD CAM combine

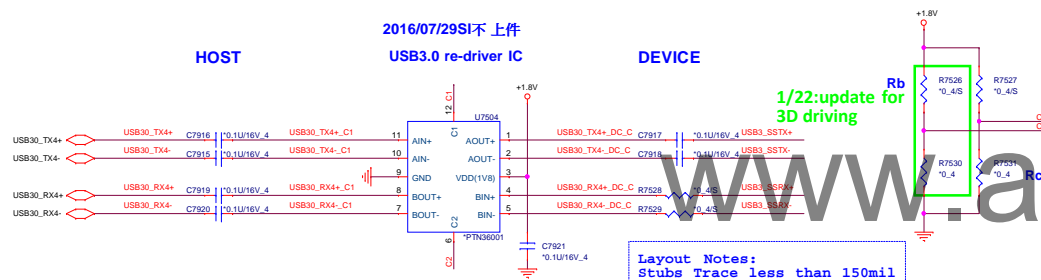
USB3.0 USB3.0 Re-driver IC

HOST

2016/07/29SI不上件
USB3.0 re-driver IC

DEVICE

1/22:update for
3D driving

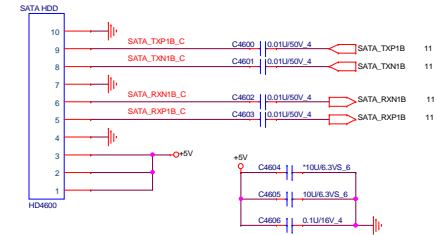


State	Channel type	Pin C1 state	Channel B	Channel A	
			EQ(3)	DE(3)	OS(3)
H	Long	H	9 dB	-5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	-3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

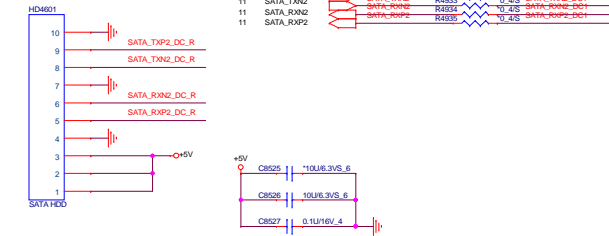
State	Channel type	Pin C2 state	Channel A	Channel B	
			EQ(3)	DE(3)	OS(3)
H	Long	H	9 dB	-5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	-3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

26,38,39,40,41,42,43,44,45,46,47,48,49,50,52
+5V
26,27,28,29,30,46,49
+5V
5,9,10,11,12,13,14,16,17,18,22,26,27,28,29,30,33,34,35,36,37,38,43,46,50,51

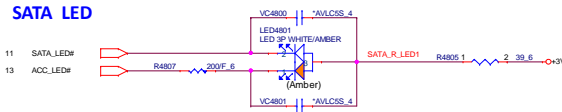
HDD



HDD (Close to ODD)



SATA LED

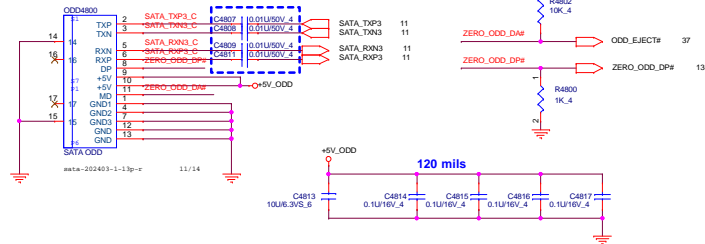


SATA_TXP2.DC1 C4624 0.01uF/50V_4
SATA_TXN2.DC1 C4625 0.01uF/50V_4
SATA_RXN2.DC1 C4626 0.01uF/50V_4
SATA_RXP2.DC1 C4627 0.01uF/50V_4


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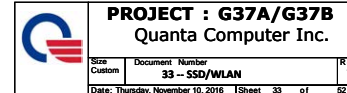
SATA ODD

Bypass CAP close CON



ZERO_PWR_ODD:
High : ODD power down
Low : ODD power on

	PROJECT : G37A/G37B		
	Quanta Computer Inc.		
	Size Custom	Document Number 32 - HDD/ODD	Rev 1A
	Date: Thursday, November 10, 2016 Sheet 32 of 52		



PN:AL009665K01



LAN & RJ45

For SWR mode support RTL8111HSH/RTL8107ESH

Stuff La,Ca,Cb

* Place Cc,Cd,Ce,Cf for RTL8111H(S) & RTL8107E(S)
close to each VDD10 pin-- 3, 22, 8, 30

* Place Cg,Ch for RTL8111H(S) & RTL8107E(S)
close to each VDD10 pin-- 22(reserved)

Power trace Layout 寬 > 60mil

La

Ca

Cb

Cc

Cd

Ce

Cf

Cg

Ch

Ci

Cj

Ck

Cl

Cm

Cn

Co

Cp

Cq

Cr

Cs

Ct

Cu

Cv

Cw

Cx

Cy

Cz

Da

Db

Dc

De

Df

Dg

Dh

Di

Dj

Dk

Dl

Dm

Dn

Do

Dp

Dq

Dr

Ds

Dt

Du

Dv

Dw

Dx

Dy

Dz

Ea

Eb

Ec

Ed

Ee

Ef

Ed

Eg

Ec

El

Ed

Em

Ed

En

Ed

EO

Ed

EP

Ed

EQ

Ed

ER

Ed

ES

Ed

ET

Ed

EU

Ed

EV

Ed

EW

Ed

EX

Ed

EY

Ed

EZ

Ed

FA

Ed

FB

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FC

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FD

Ed

FE

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FG

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FH

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FI

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FJ

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FK

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JQ

Ed

JR

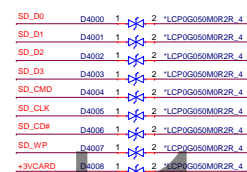
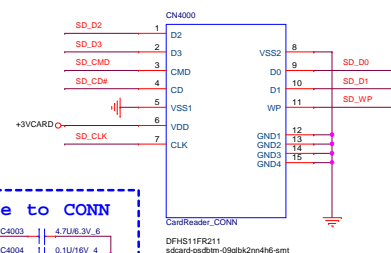
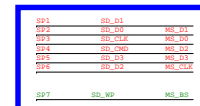
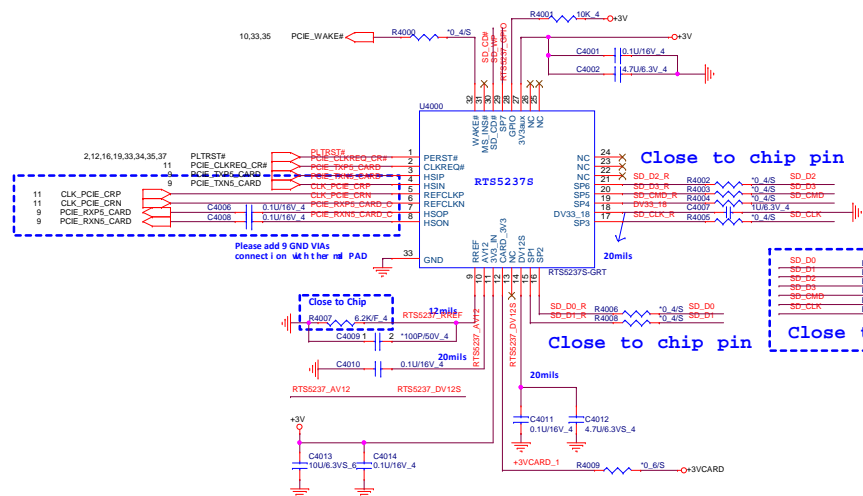
Ed

JS

Ed

JT

Ed



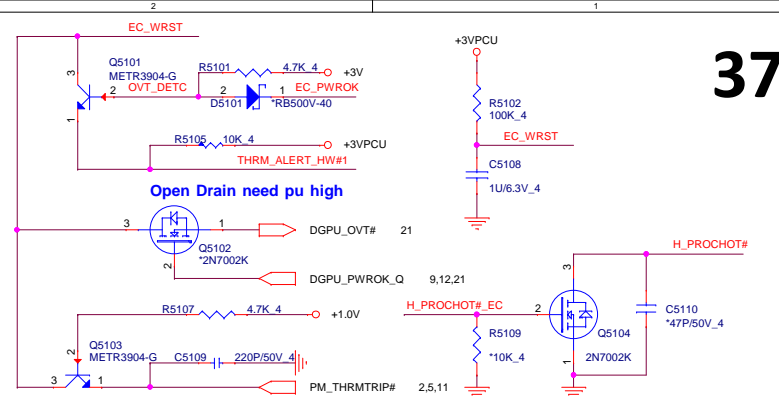
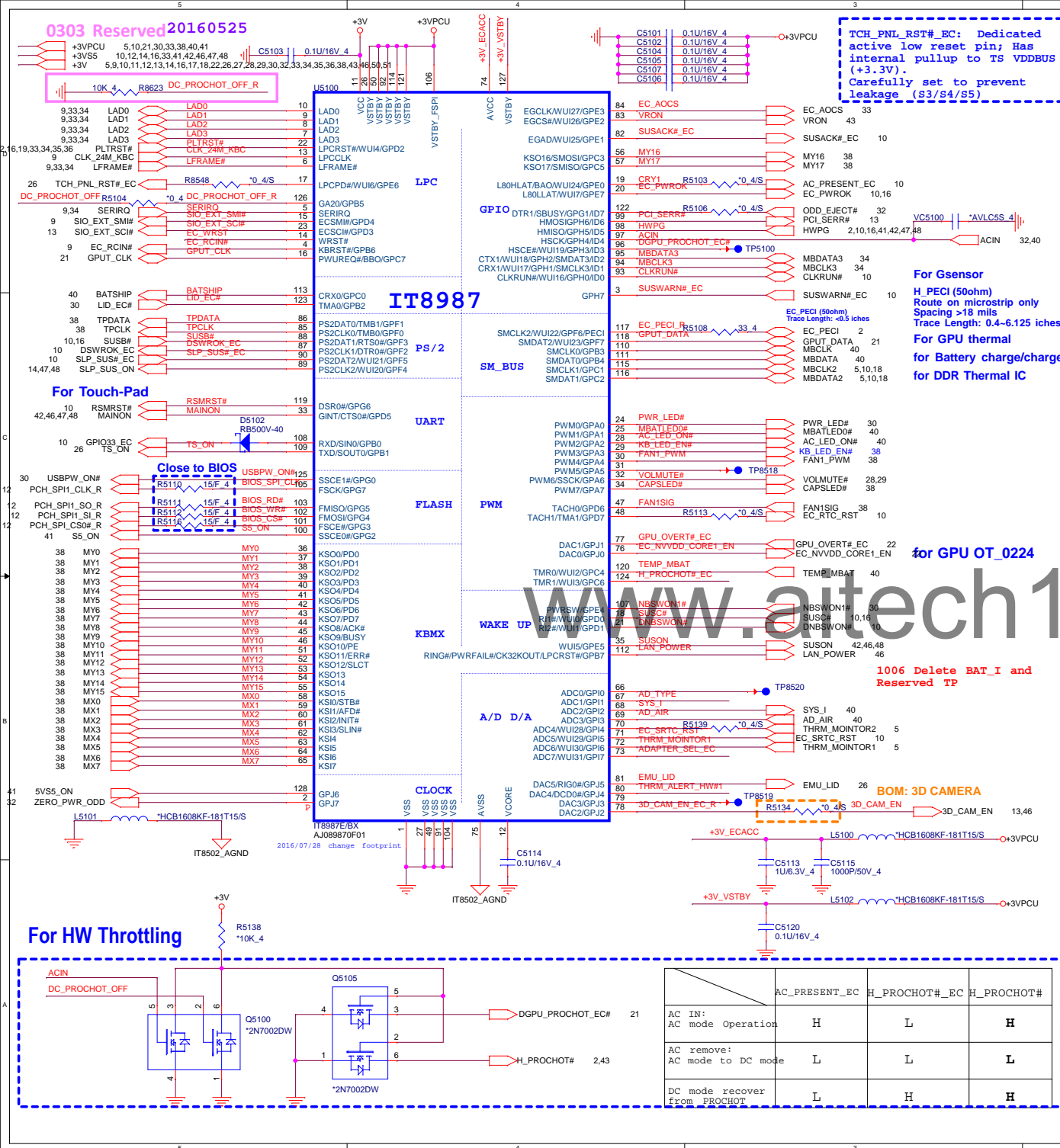
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PROJECT : G37A/G37B
Quanta Computer Inc.

Size Custom	Document Number 36 - CR RTS5237S/CR SOCKET
Date: Thursday, November 10, 2016 Sheet: 36 of 52	

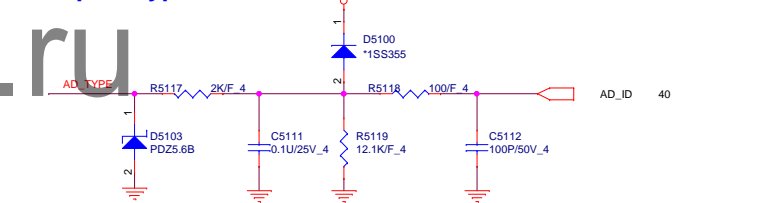
0303 Reserved 20160525



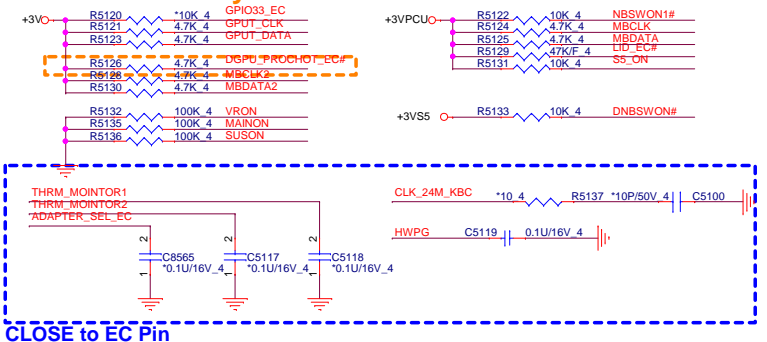
Adapter select for EC

	Ra	Rb	ADAPTER_SEL_EC	BOM
200W	10K(CS31002FB26)	100K (CS41002FB28)	3V	
150W	10K(CS31002FB26)	27.4K(CS32742FB14)	2.42V	
120W	10K(CS31002FB26)	12.1K(CS31212FB28)	1.8V	DIS
90W	10K(CS31002FB26)	6.2K(CS26202FB17)	1.26V	UMA
65W	10K(CS31002FB26)	2.2K(CS22202FB08)	0.59V	
45W	NC	10K(CS31002FB26)	0V	

Adapter Type check



BOM:DIS only

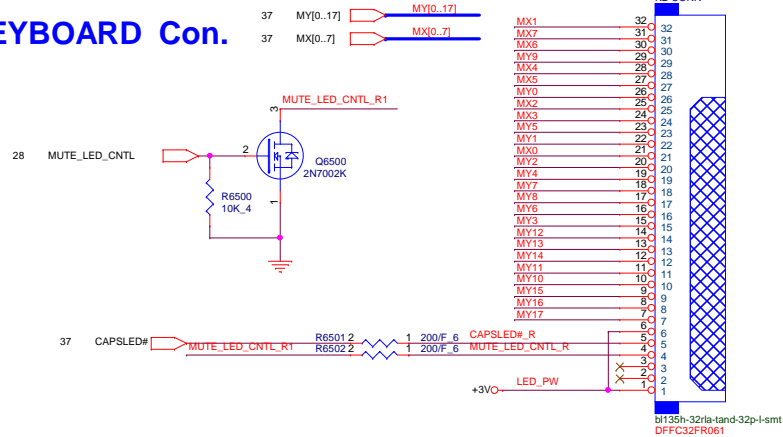


PROJECT : G37A/G37B
Quanta Computer Inc.

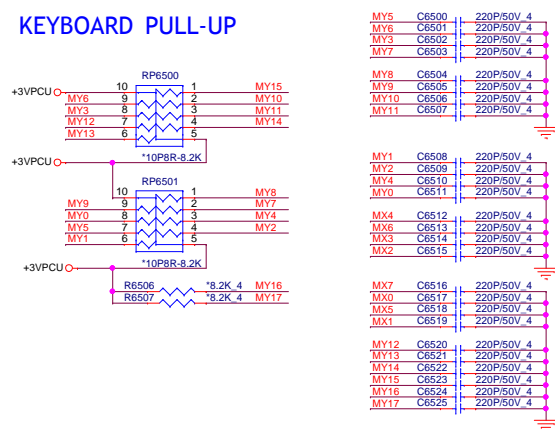
Size	Document Number	Rev
Custom	37 -- EC (IT8987)	1A
Date: Thursday, November 10, 2016	Sheet 37 of 52	

+VIN	26,32,39,40,41,42,43,44,45,46,47,48,49,50,52
+5V	26,27,28,29,32,46,49
+3VPCU	5,10,21,30,33,37,40,41
+3VS5	10,12,14,16,33,37,41,42,46,47,48
+3VSUS	46
+3V	5,9,10,11,12,13,14,16,17,18,22,26,27,28,29,30,32,33,34,35,36,37,43,46,50,51

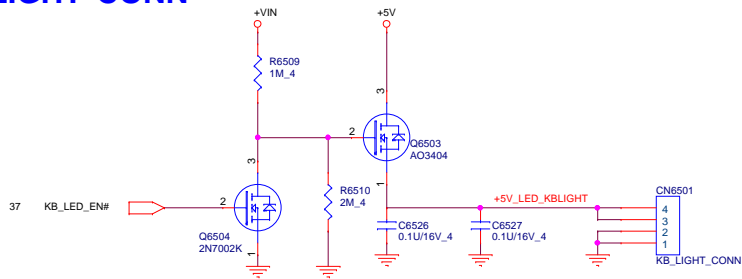
KEYBOARD Con.



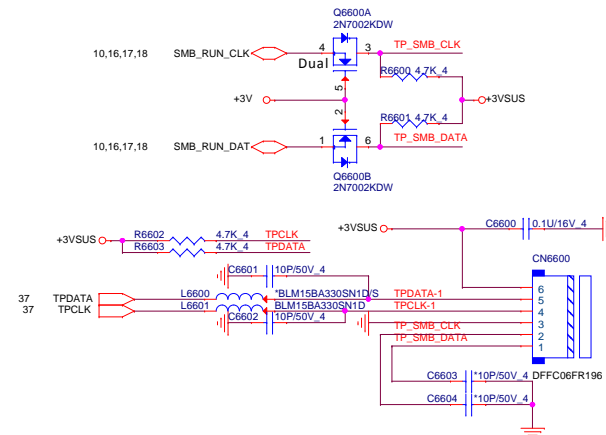
KEYBOARD PULL-UP



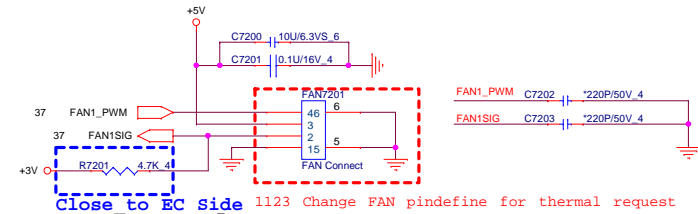
KB LIGHT CONN



Touch Pad Connector

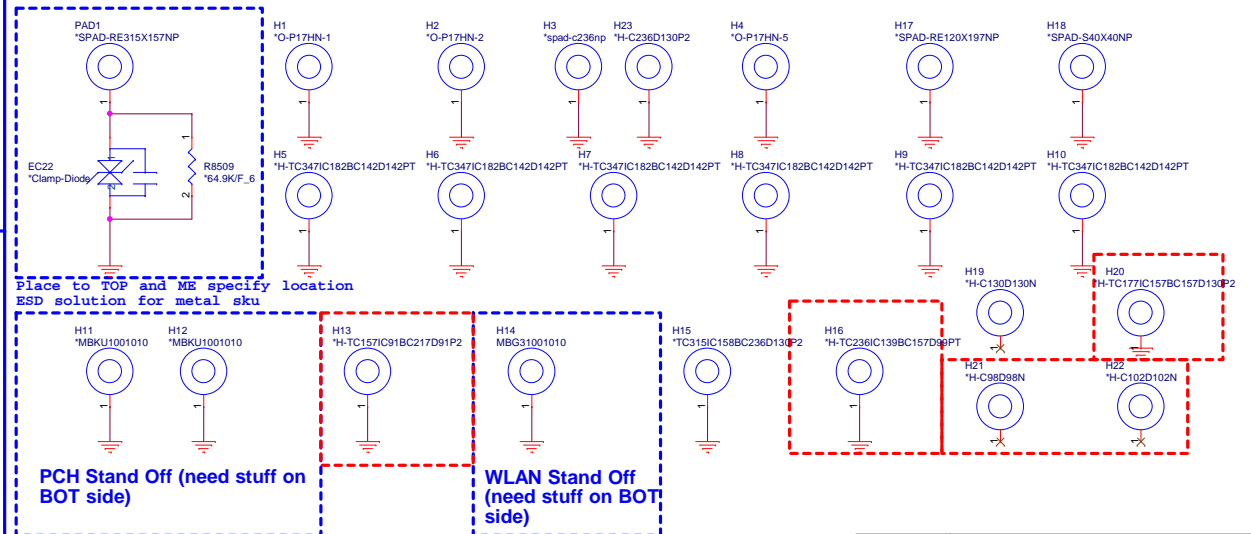


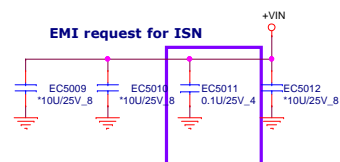
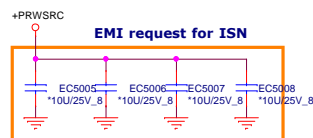
FAN



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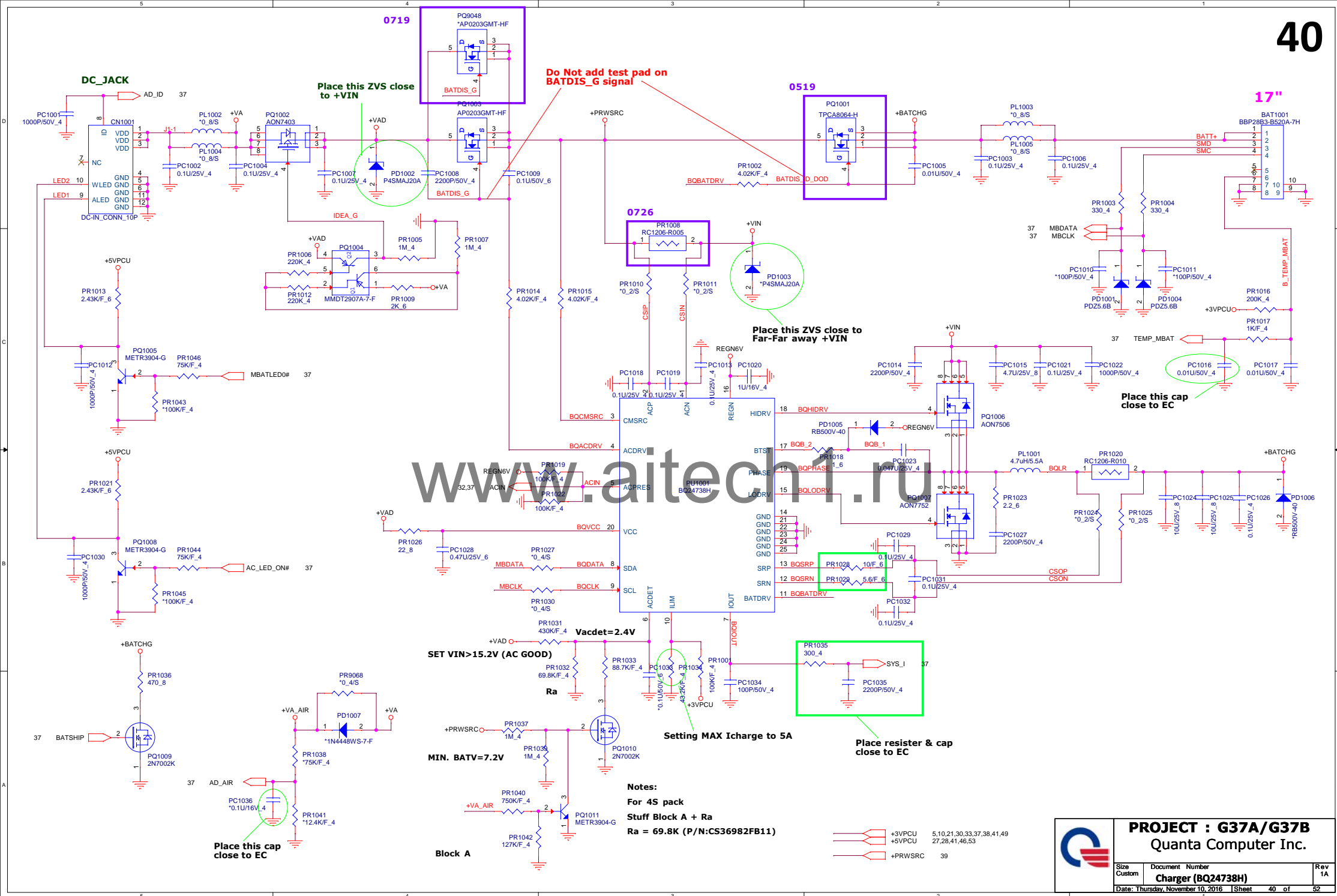
HOLE

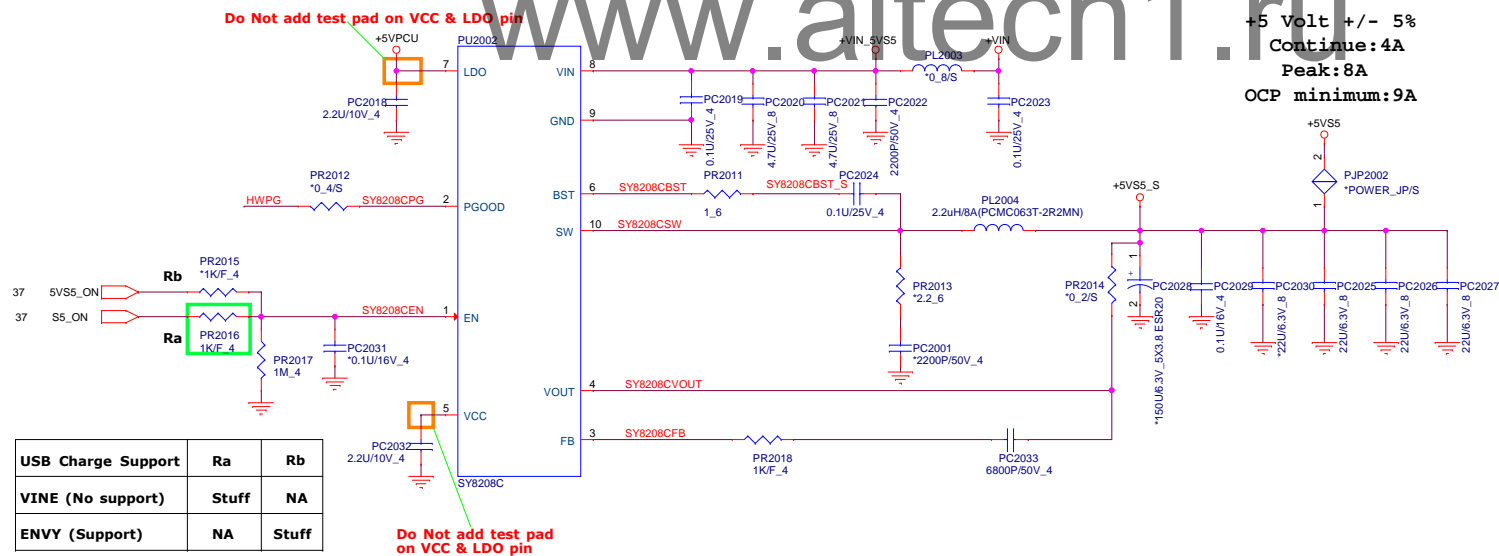
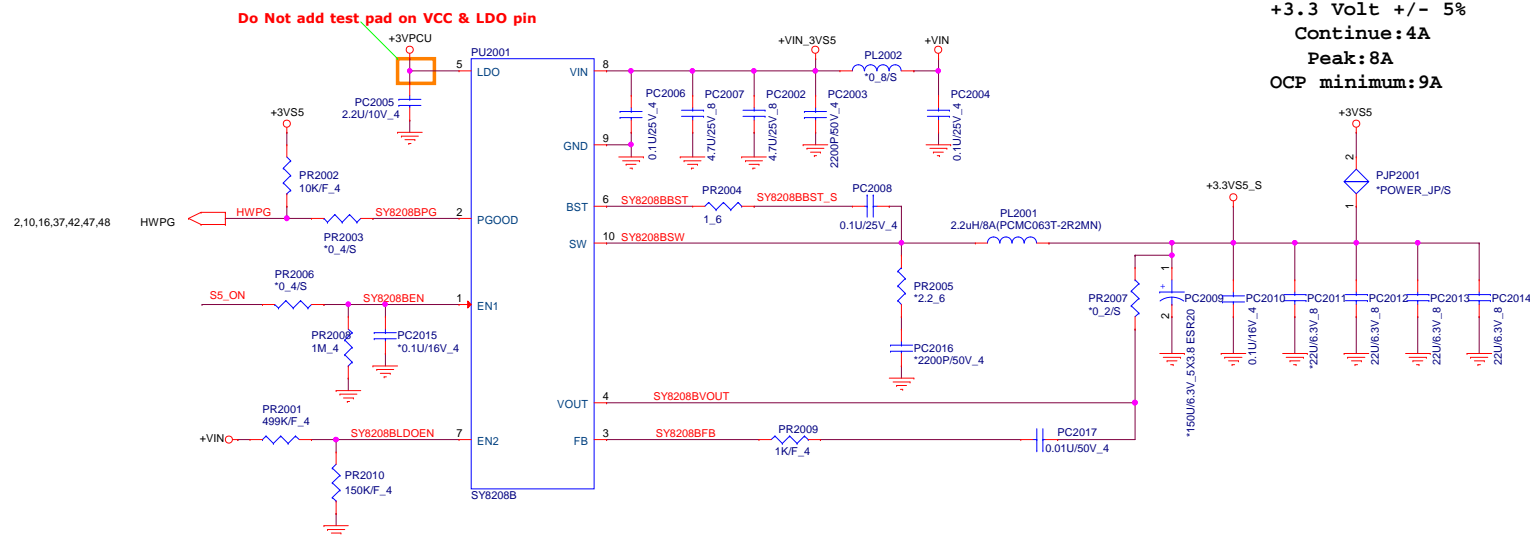




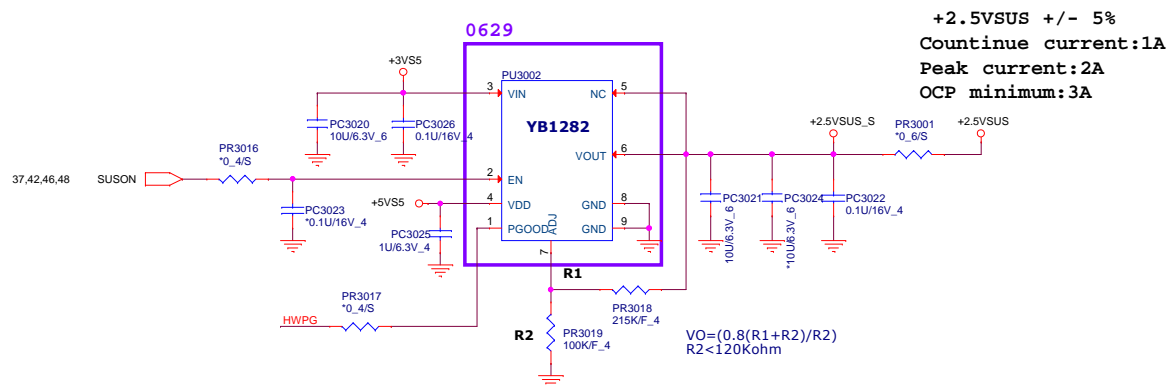
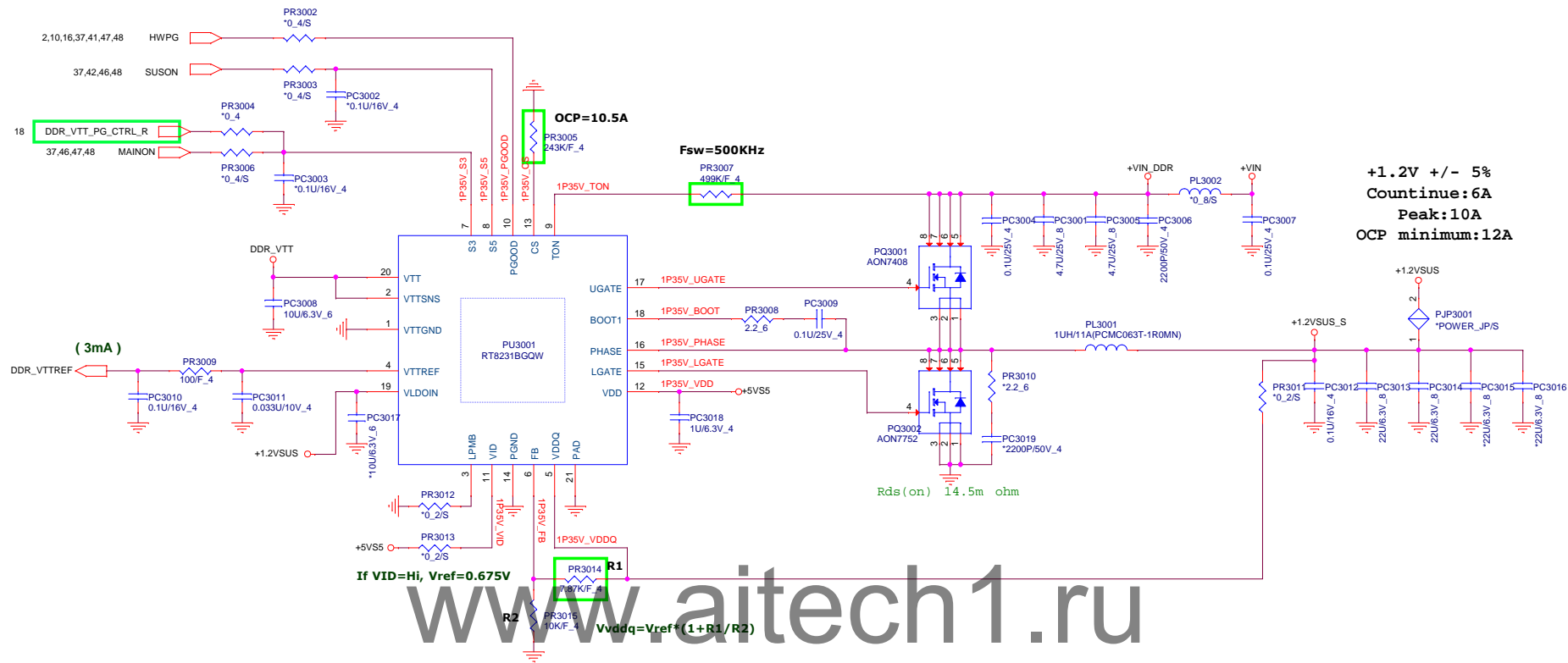
20160308 MV change for EMI request

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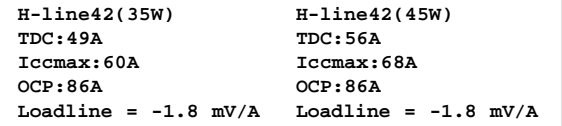


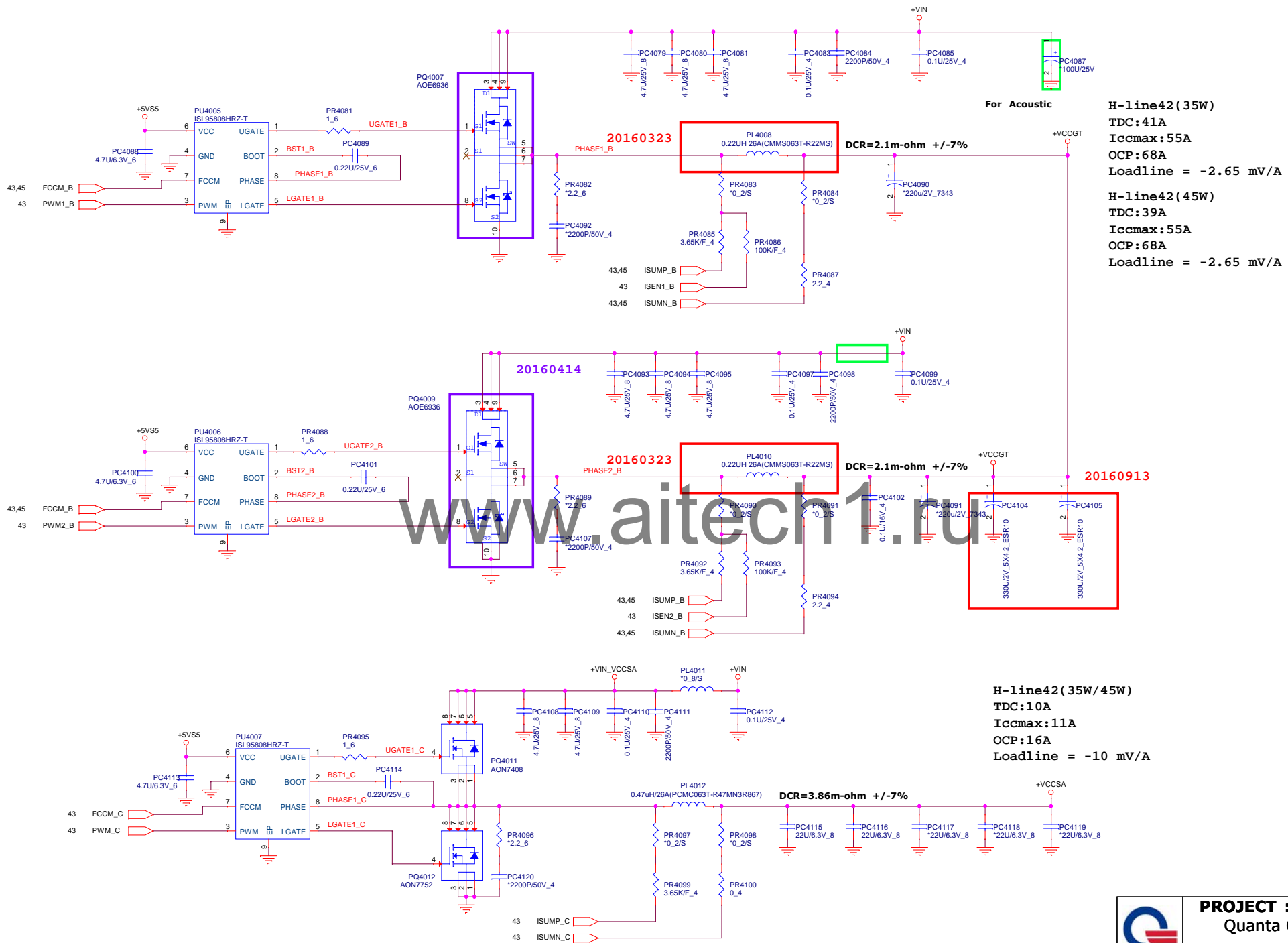
+VIN 26,32,38,39,40,42,43,44,45,46,47,48,49,52
 +3VS5 10,12,14,16,26,33,37,42,46,47,48
 +5VS5 10,26,28,30,42,43,44,45,46,47,48,49,50,51,52,53
 +3VPCU 5,10,21,30,33,37,38,40,49
 +5VPCU 27,28,40,46,53

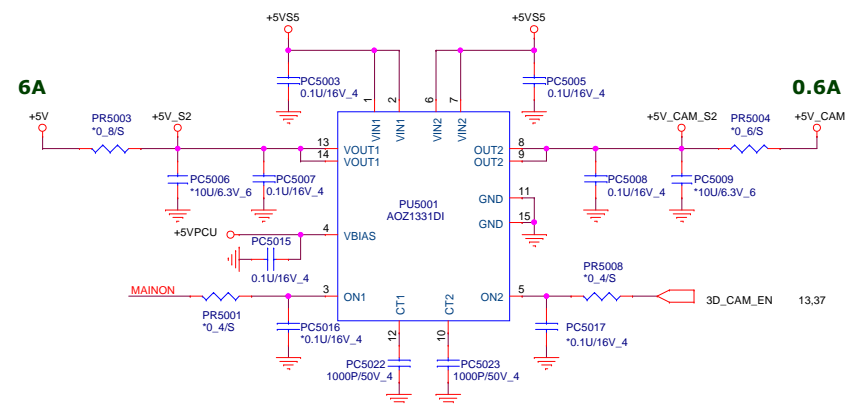
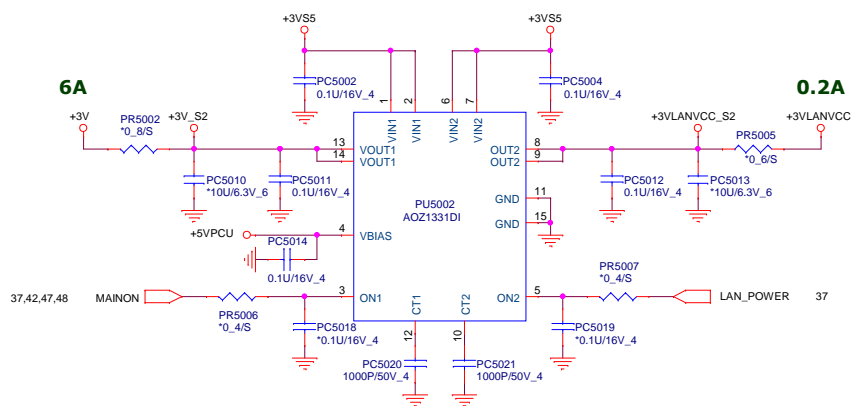


+VIN	26,32,38,39,40,41,43,44,45,46,47,48,49,52
+5VS5	10,26,28,30,41,43,44,45,46,47,48,49,50,51,52,53
+1.2VSUS	2,6,10,17,18,48,53
DDR_VTT	17,18
+2.5VSUS	17,18

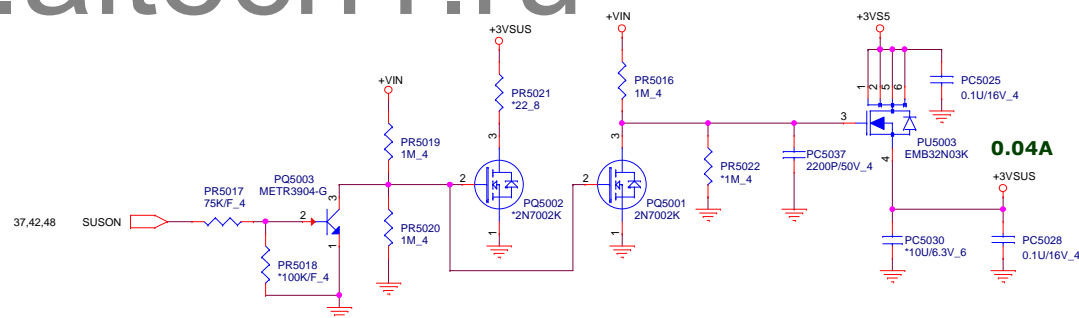
 PROJECT : G37A/G37B Quanta Computer Inc.		
Size	Document Number	Rev
	DDR3 (RT8231B)	1A
Thursday, November 10, 2016	Sheet 42	of 52



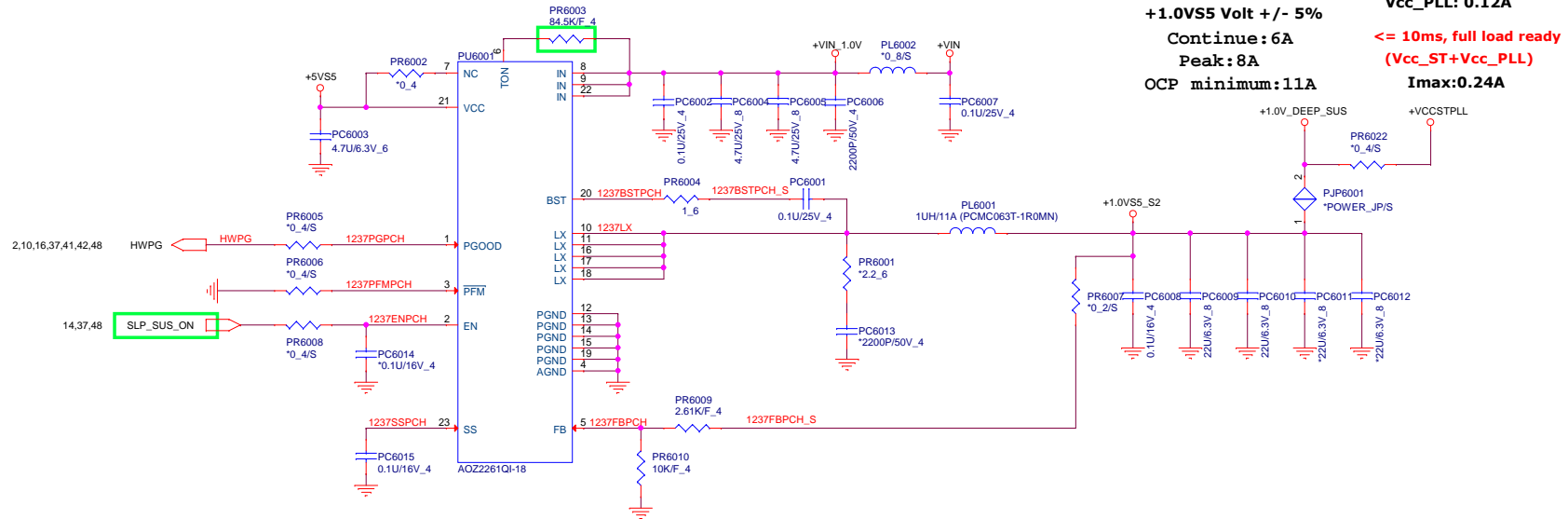




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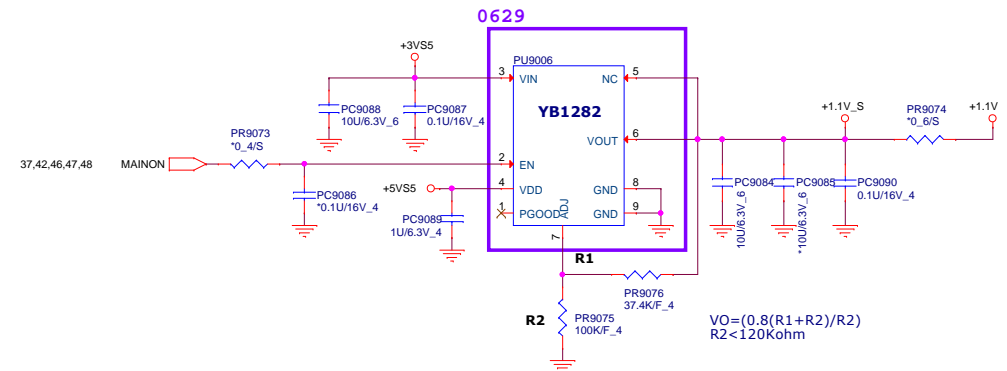
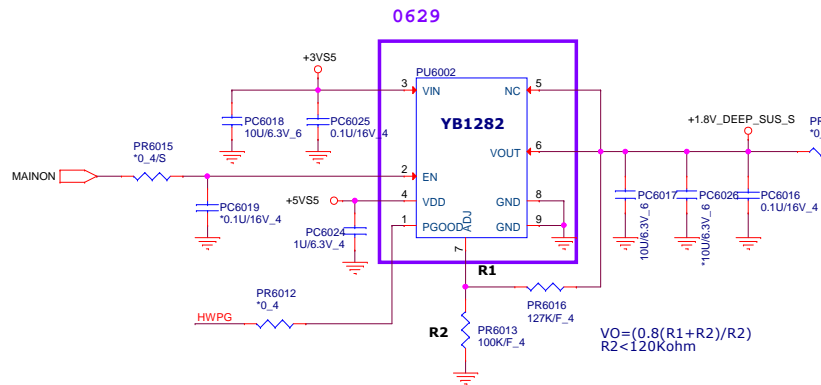
+3V	5,9,10,11,12,13,14,16,17,18,26,27,28,29,30,32,33,34,35,36,37,38,43,52
+5V	26,27,28,29,31,32,38
+3VS5	10,12,14,16,26,33,37,41,42,47,48
+5VS5	10,26,28,30,41,42,43,44,45,47,48,49,50,51,52,53
+3VSUS	38
+3VLAVCC	27,35
+5V_CAM	31
+3V_DEEP_SUS	9,10,12,13,14,16,18



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+1.1V +/- 5%
TDC: 1A
EDP: 2A

+1.8V +/- 5%
TDC: 1A
EDP: 2A



+VIN 26,32,38,39,40,41,42,43,44,45,46,48,49,52
+3VS5 10,12,14,16,26,33,37,41,42,46,48
+5VS5 10,26,28,30,41,42,43,44,45,46,48,49,50,51,52,53
+1.0V_DEEP_SUS 10,11,14,16,48
+1.8V 28,31,53
+VCCSTPLL 2,6,43

Volume Segment

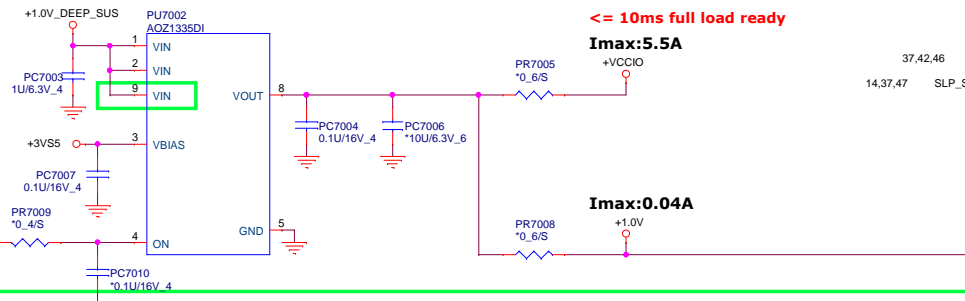
Vcc_STG: 0.04A

Vcc_IO: 5.5A

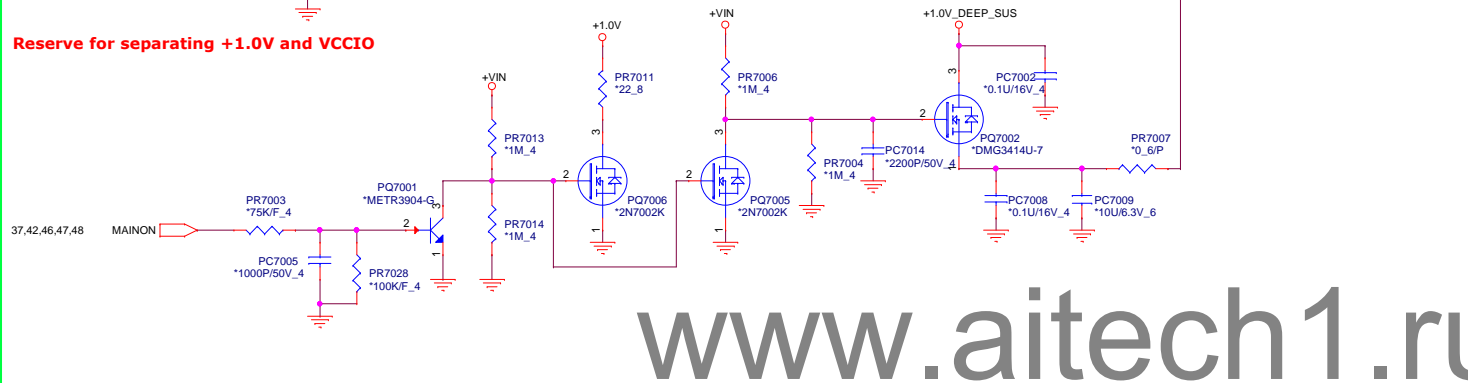
<= 10ms full load ready

Imax:5.5A

Imax:0.04A

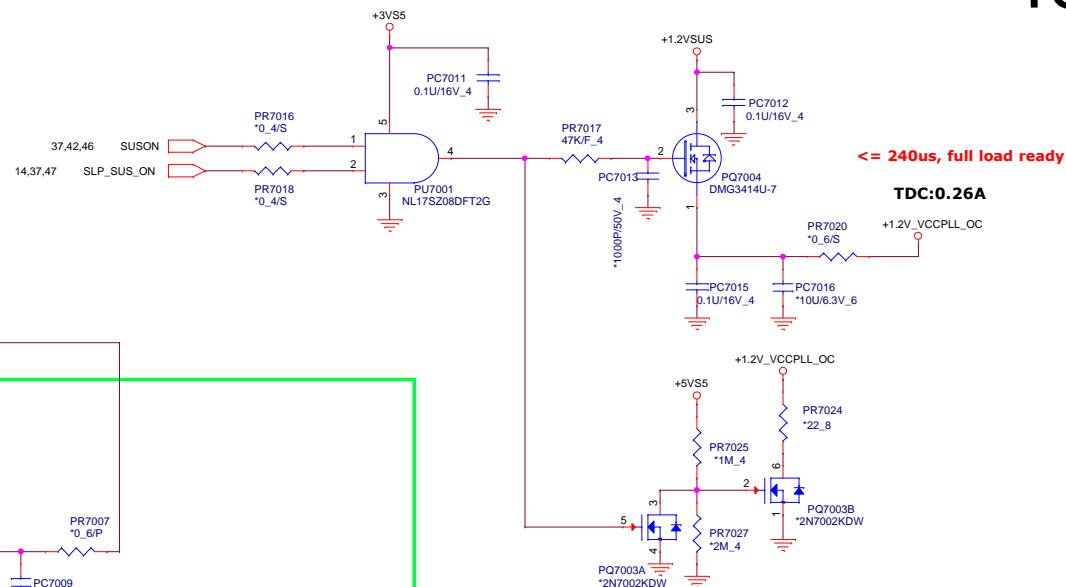
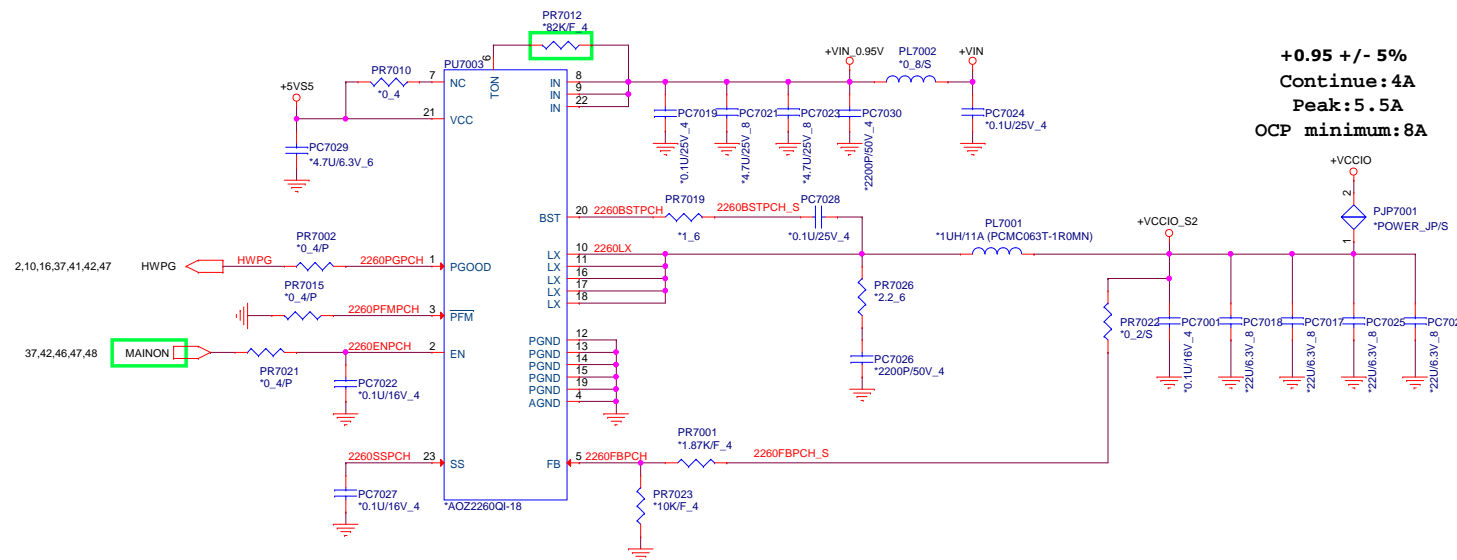


Reserve for separating +1.0V and VCCIO



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+0.95 +/- 5%
Continue: 4A
Peak: 5.5A
OCP minimum: 8A



<= 240us, full load ready

TDC:0.26A

+1.0V	2,5,6,10,16,37
+3VS5	10,12,14,16,26,33,37,41,42,46,47
+5VS5	10,26,28,30,41,42,43,44,45,46,47,48,50,51,52,53
+VCCIO	3,6,16
+1.0V_DEEP_SUS	10,11,14,16,47
+1.2V_VCCPLL_OC	6
+1.2VSUS	2,6,10,17,18,42,53



PROJECT : G37A/G37B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V/+VCCSTPLL+VCCIO	1A

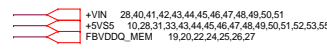
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NVDDS

1. **Ripple Current:**
 $I_{rip}=7.79A$
2. **Ripple Voltage:**
 $ESR/1s=9m\Omega$
 $V_{rip}=70.11mV$
3. **MOSFET Spec:**
L-side MOSFET: FDCPC5030
 $R_{ds}(ON)=3m\Omega$ ($V_{gs}=4.5V$)
 $I_{cont}=25A$ ($T=25^{\circ}C$)
 $I_{pulse}=503A$
4. **Frequency:**
 $F=500KHz$ ($PR2924=300k\Omega$)
5. **OCF:**
Set = PR9008 to 14.7K
 $V_{trip} = PR9008 \cdot 10uA \cdot 40mV = 107V$
 $V_{trip} = (V_{trip}/R_{ds(on)} + I_{ripple}/2$
 $= 39.565A$ (1 phase)

Total OCF= $39.565 \cdot 3=118.7A$ (3 phase)

N17P-G1 (50W) /N17P-G0(40W)
EDP-C: 47A/40A
EDP-P: 90A/85A
OCP minimum: 108A/103A



1. Ripple Current:
 Irp=5.34A Vo=1.35V
 Irp=5.88A Vo=1.5V

2. Ripple Voltage:
 ESR/1=9mohm
 Vrip=48.06mV Vo=1.35
 Vrip=53mV Vo=1.5





3.MOSFET Spec:
 L-side MOSFET: FDMOS3669S
 Rds(on)=2.2mohm (Vgs=4.5 V)
 I cont = 18A (T=25 °C)
 I pulse=60A

4. Frequency:
 F=500KHz (PR9145=300k ohm)





5. OCP:
 Set = PR9147 to 133K Vo=1.35
 Vtrip= PR9147*10uA/12=110.83mV
 locp=(Vtrip/Rds(on) + Irripple/2 = 24A

MEM_VDD_CTRL	FBVDDQ_MEM
1	1.5V
0	1.35V



	+VIN	26,32,38,39,40,41,42,43,44,45,47,48,49,50
	+3VS5	10,12,14,16,26,33,37,41,42,46,47,48
	+5VS5	10,26,28,30,41,42,43,44,45,46,47,48,49,50
	+1.2VSUS	2,6,10,17,18,42,46,48



	+VIN	26,32,38,39,40,41,42,43,44,45,47,48,49,50
	+3VS5	10,12,14,16,26,33,37,41,42,46,47,48
	+5VS5	10,26,28,30,41,42,43,44,45,46,47,48,49,50
	+1.2VSUS	2,6,10,17,18,42,46,48



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